LAB MANUAL

PULSE CIRCUITS AND ICs LAB
EC-361

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1. Linear Wave Shaping

Aim:

i) To design a low pass RC circuit for the given cutoff frequency and obtain its frequency response.

ii) To observe the response of the designed low pass RC circuit for the given square waveform for T<<RC,T=RC and T>>RC.

iii) To design a high pass RC circuit for the given cutoff frequency and obtain its frequency response.

iv) To observe the response of the designed high pass RC circuit for the given square waveform for T<<RC, T=RC and T>>RC.

Apparatus Required:

Name of the Component/Equipment	Specifications	Quantity
Resistors	1KΩ	1
	2.2KΩ,16 KΩ	1
Capacitors	0.01μF	1
CRO	20MHz	1
Function generator	1MHz	1

Theory:

The process whereby the form of a non sinusoidal signal is altered by transmission through a linear network is called “linear wave shaping”. An ideal low pass circuit is one that allows all the input frequencies below a frequency called cutoff frequency f_c and attenuates all those above this frequency. For practical low pass circuit (Fig.1) cutoff is set to occur at a frequency where the gain of the circuit falls by 3 dB from its maximum at very high frequencies the capacitive reactance is very small, so the output is almost equal to the input and hence the gain is equal to 1. Since circuit attenuates low frequency signals and allows high frequency signals with little or no attenuation, it is called a high pass circuit.

Circuit Diagram:

Low Pass RC Circuit :

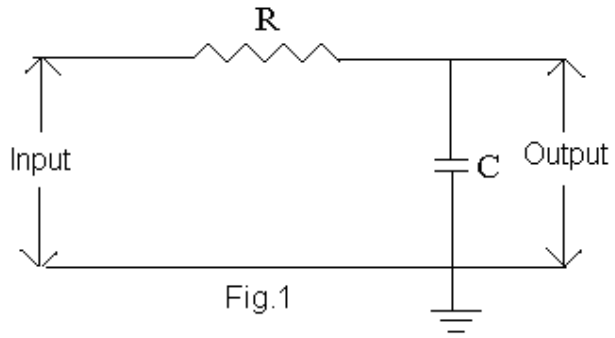


Fig.1

High Pass RC Circuit :

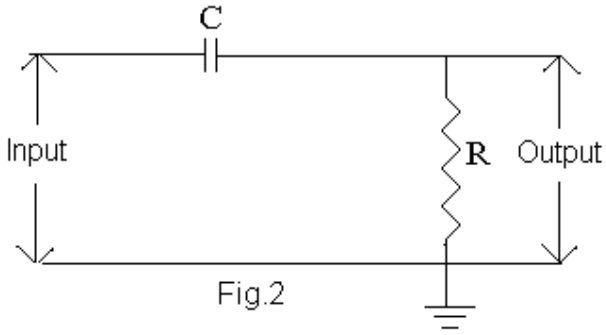


Fig.2

Procedure:

A) Frequency response characteristics:

1 .Connect the circuit as shown in Fig.1 and apply a sinusoidal signal of amplitude of 2V p-p as input.

2. Vary the frequency of input signal in suitable steps 100 Hz to 1 MHz and note down the p-p amplitude of output signal.

3. Obtain frequency response characteristics of the circuit by finding gain at each frequency and plotting gain in dB vs frequency.

4. Find the cutoff frequency f_c by noting the value of f at 3 dB down from the maximum gain

B) Response of the circuit for different time constants:

Time constant of the circuit RC= 0.0198 ms

1. Apply a square wave of 2v p-p amplitude as input.
2. Adjust the time period of the waveform so that T>>RC, T=RC,T<<RC and observe the output in each case.
3. Draw the input and output wave forms for different cases.

Sample readings

Low Pass RC Circuit Input Voltage: V_i=2 $V_{(p-p)}$

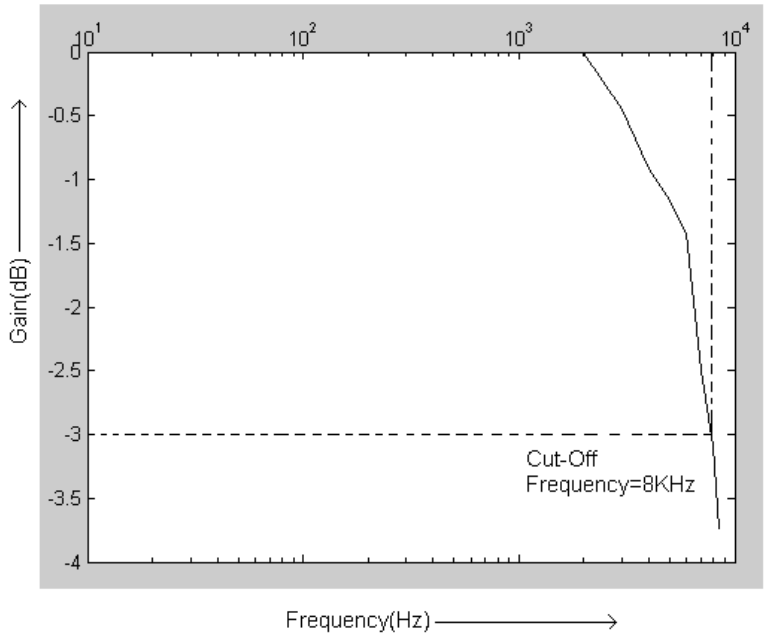
S.No	Frequency (Hz)	O/P Voltage, V_o (V)	Gain = 20log(Vo/Vi) (dB)

High Pass RC Circuit:

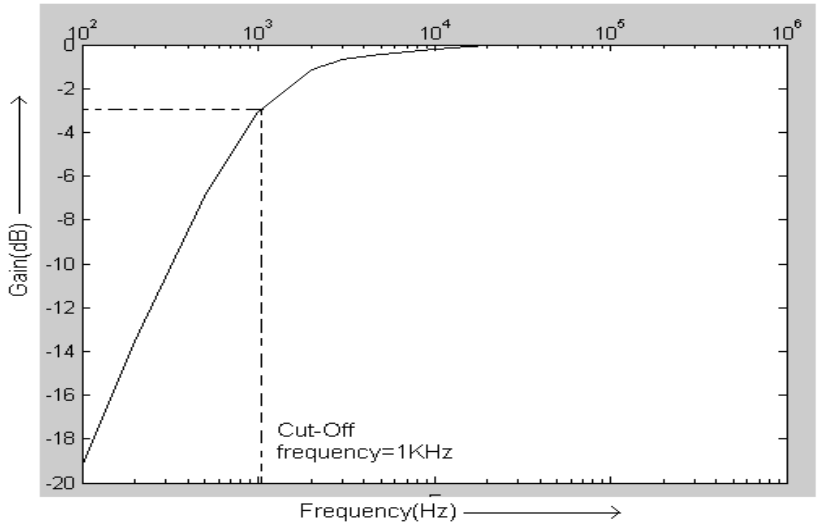
S.No	Frequency (Hz)	O/P Voltage, V_o (V)	Gain = 20log(Vo/Vi) (dB)

Model Graphs and wave forms

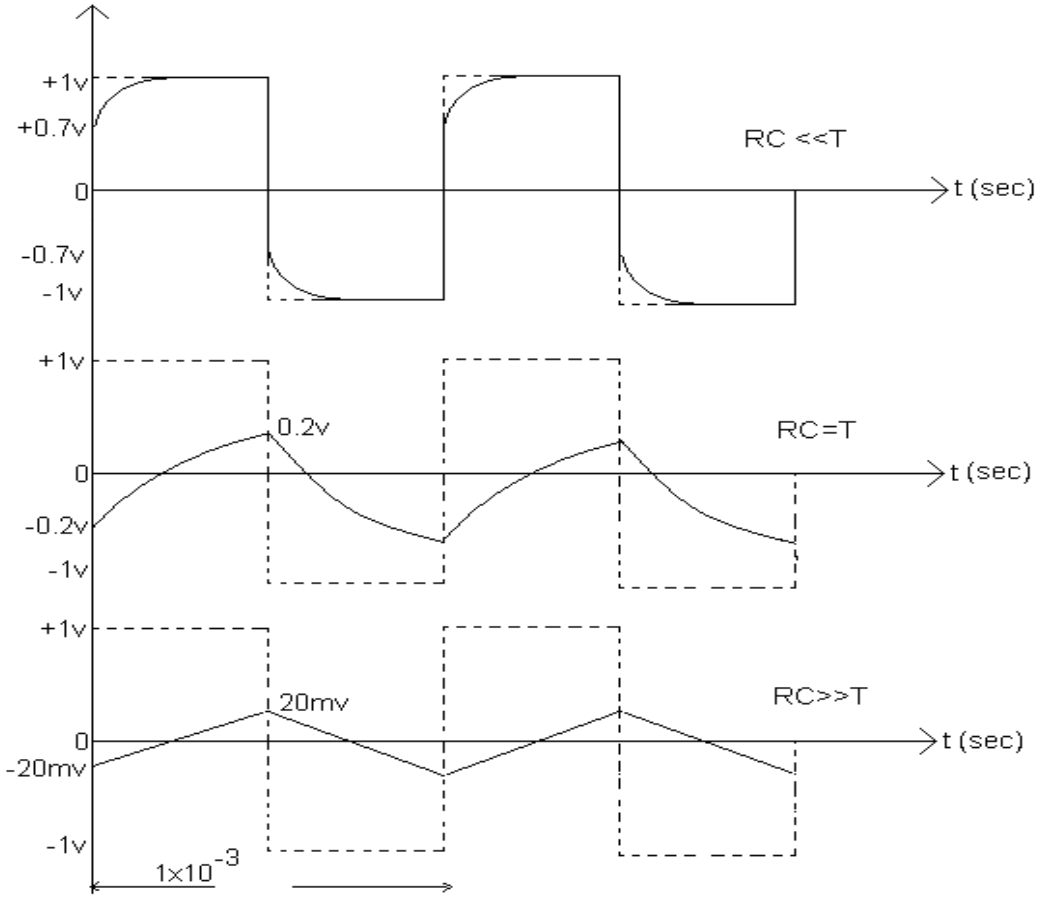
Low Pass RC circuit frequency response:



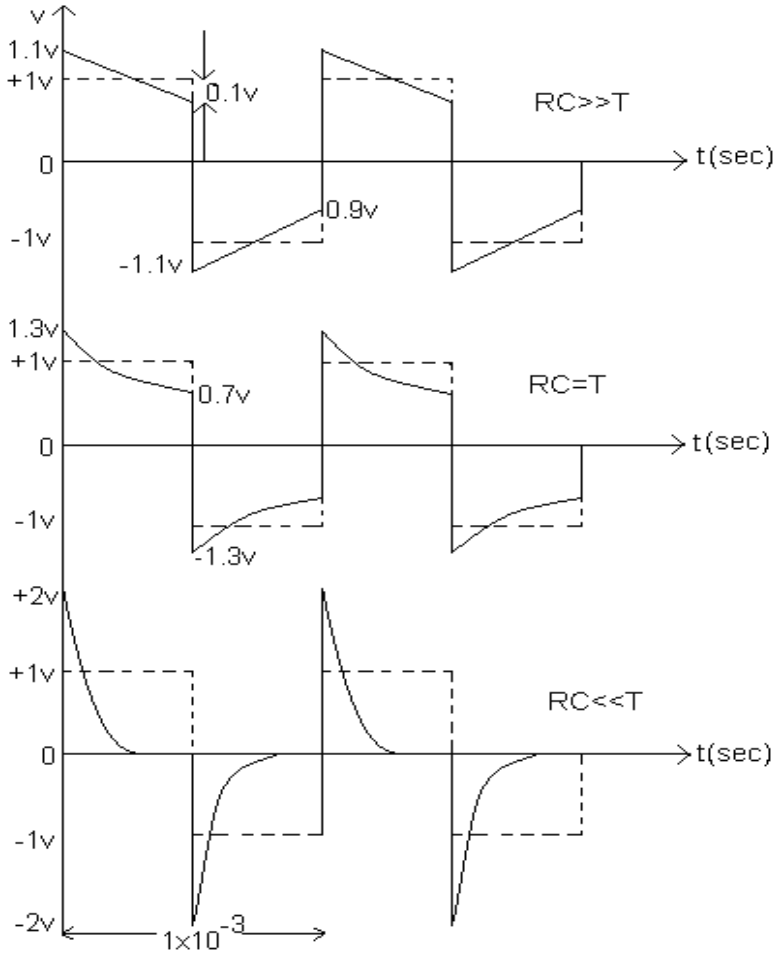
High Pass RC circuit frequency response:



Low Pass RC circuit



High Pass RC Circuit



Precautions:

1. Connections should be made carefully**.**
2. Verify the circuit connections before giving supply.
3. Take readings without any parallax error.

Result: RC low pass and high pass circuits are designed, frequency response and response at different time constants is observed.

Inference: At low frequencies the capacitor C behaves almost like a open circuit and output is equal to input voltage. As the frequency increases the reactance of the capacitor increases and C functions almost like a short circuit and output voltage is equal to zero. So the low pass RC allows low frequency signals and stops high frequency signals. When the time constant of the circuit is less than the time period of a input signal, the capacitor charges and discharges quickly. So the shape of the output is same as the input signal. But as the time constant of circuit is increases the capacitor charges and discharges very slowly so when the time constant of the low pass RC circuit is very much greater than the time period of a input signal it acts as a integrator.

2(a). Non Linear Wave Shaping-Clippers

Aim: To obtain the output and transfer characteristics of various diode clipper circuits.

Apparatus required:

Name of the Component/Equipment	Specifications	Quantity
Resistors	1KΩ	1
Diode	1N4007	1
Cathode Ray Oscilloscope	20MHz	1
Function generator	1MHz	1
Regulated power supply	0-30V,1A	1

Theory:

The basic action of a clipper circuit is to remove certain portions of the waveform, above or below certain levels as per the requirements. Thus the circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform are called clipper circuits or Clippers. The half wave rectifier is the best and simplest type of clipper circuit which clips off the positive/negative portion of the input signal. The clipper circuits are also called limiters or slicers.

Circuit diagrams:

Positive peak clipper with reference voltage, V=2V

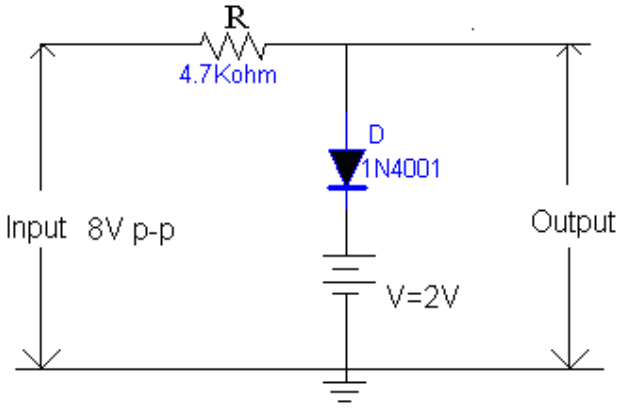


Fig.1

Positive Base Clipper with Reference Voltage, V=2V

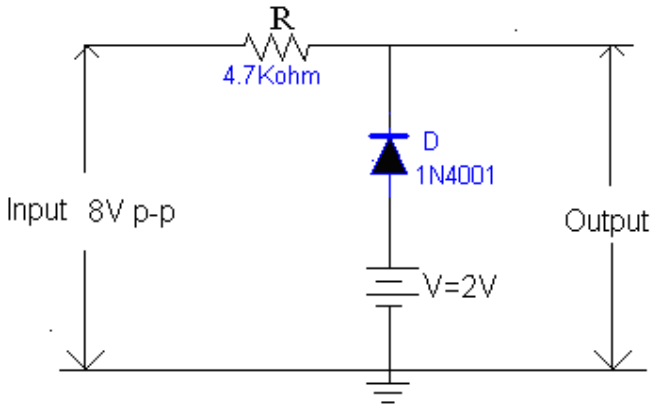


Fig.2

Negative Base Clipper with Reference Voltage,V=-2V

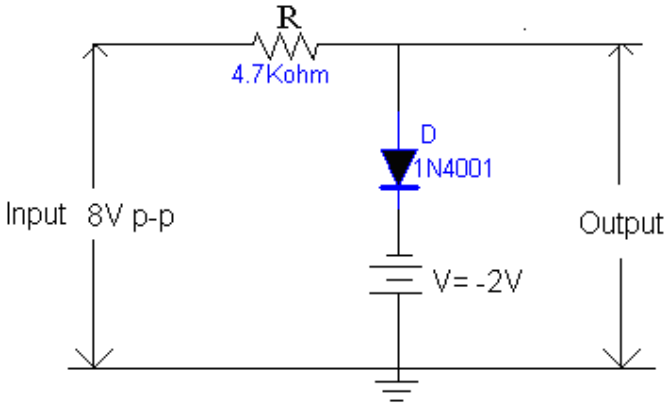


Fig.3

Negative peak clipper with reference voltage, V=-2v

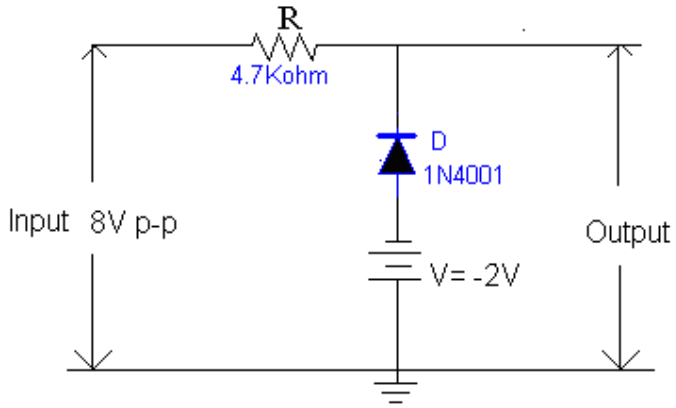


Fig.4

Slicer Circuit:

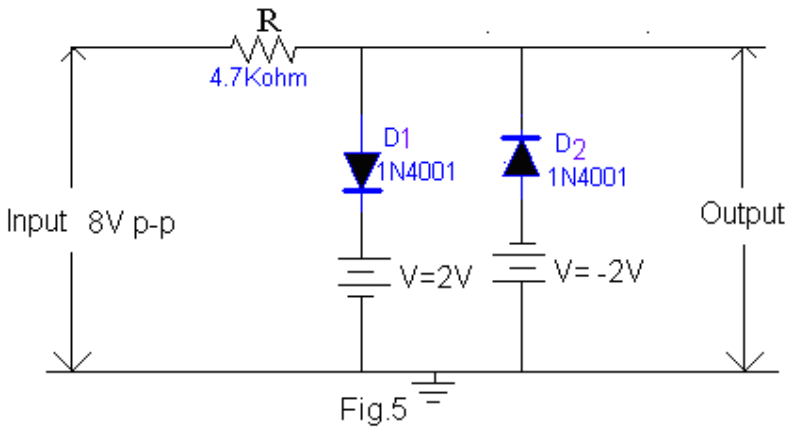


Fig.5

Procedure:

1. Connect the circuit as per circuit diagram shown in Fig.1
2. Obtain a sine wave of constant amplitude 8 V p-p from function generator and apply as input to the circuit.
3. Observe the output waveform and note down the amplitude at which clipping occurs.
4. Draw the observed output waveforms.
5. To obtain the transfer characteristics apply dc voltage at input terminals and vary the voltage insteps of 1V up to the voltage level more than the reference voltage and note down the corresponding voltages at the output.
6. Plot the transfer characteristics between output and input voltages.
7. Repeat the steps 1 to 5 for all other circuits.

Sample Readings:

Positive peak clipper: Reference voltage, V=2V

S.No	I/p voltage (v)	O/p voltage (v)

Positive base clipper: Reference voltage V= 2V

S.No	I/p voltage(v)	O/p voltage(v)

Negative base clipper: Reference voltage= 2V

S.No	I/p voltage(v)	O/p voltage(v)

Negative peak clipper: Reference voltage= 2 V

S.No	I/p voltage(v)	O/p voltage(v)

Slicer Circuit:

S.No	I/p voltage(v)	O/p voltage(v)

Theoretical calculations:

Positive peak clipper:

V_r=2v, Vγ=0.6v

When the diode is forward biased $V_o = V_r + V\gamma$

=2v+0.6v

= 2.6v

When the diode is reverse biased the $V_o=V_i$

Positive base clipper:

V_r=2v, Vγ=0.6v

When the diode is forward biased Vo=Vr –Vγ

= 2v-0.6v

= 1.4v

When the diode is reverse biased $V_o=V_i$.

Negative base clipper:

V_r=2v, Vγ=0.6v

When the diode is forward biased $V_o = -V_r + V\gamma$

$=-2v+0.6v$

$=-1.4v$

When the diode is reverse biased $V_o=V_i$.

Negative peak clipper:

V_r=2v, Vγ=0.6v

When the diode is forward biased $V_o= -(V_r + V\gamma)$

$= -(2+0.6)v$

$=-2.6v$

When the diode is reverse biased $V_o=V_i$.

Slicer:

When the diode D1 is forward biased and D2 is reverse biased $V_o= V_r + V\gamma$

$=2.6v$

When the diode D2 is forward biased and D2 is reverse biased $V_o=-(V_r + V\gamma)$

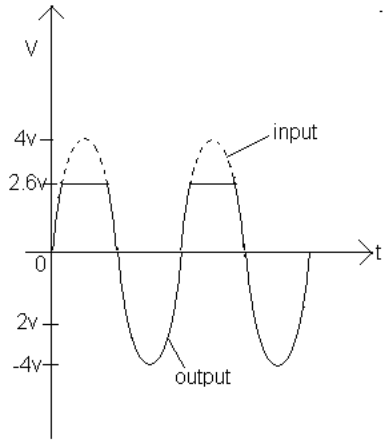
$= -(2+0.6)v$

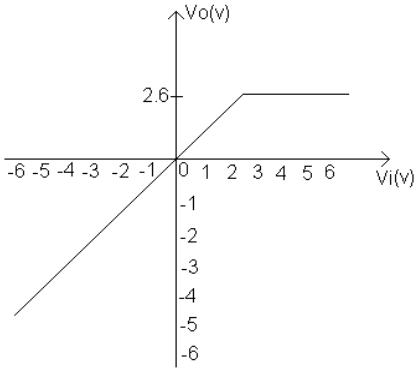
$=-2.6v$

When the diodes D1 &D2 are reverse biased $V_o=V_i$.

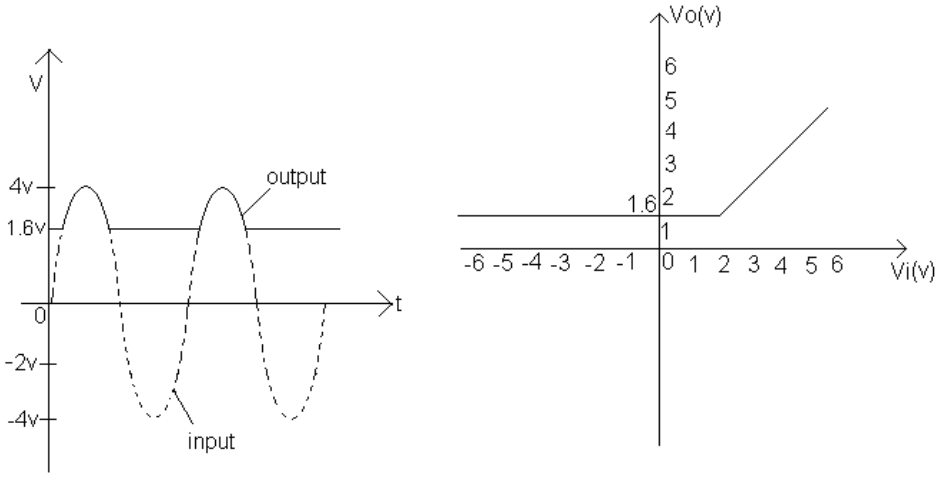
Model wave forms and Transfer characteristics

Positive peak clipper: Reference voltage= 2V

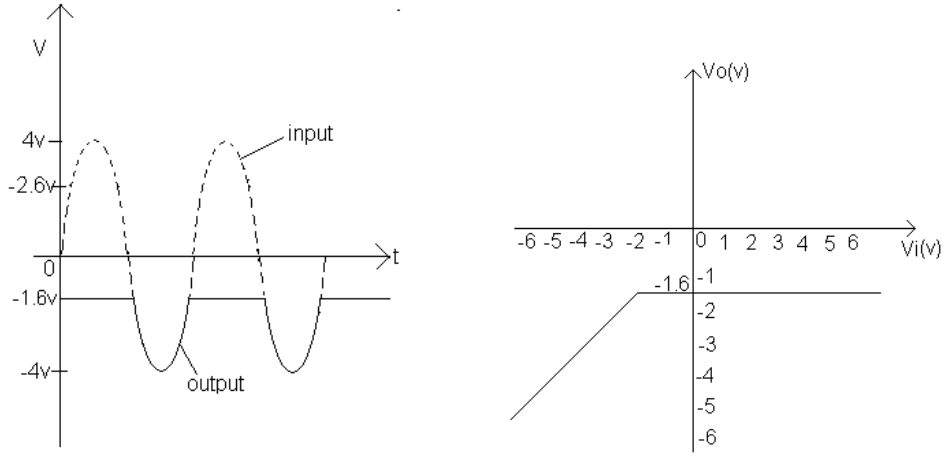




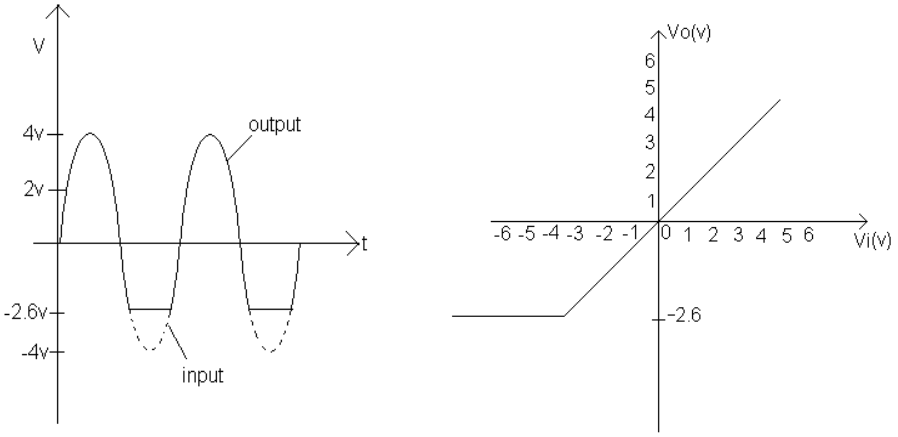
Positive base clipper: Reference voltage= 2V



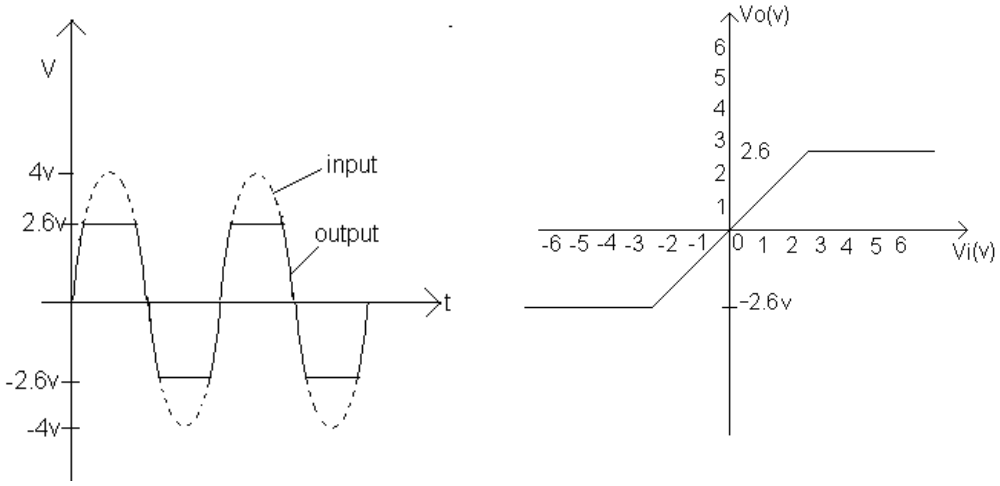
Negative base clipper: Reference voltage= 2v



Negative peak clipper: Reference voltage= 2 V



Slicer Circuit:



Precautions:

1. Connections should be made carefully**.**
2. Verify the circuit before giving supply.
3. Take readings without any parallax error.

Result:

Performance of different clipping circuits is observed and their transfer characteristics are obtained.

Inference:

The clipper circuits clips off the some part of the waveform depend on the applied reference voltage. Clipping circuits do not require energy storage elements these circuits can also used as sine to square wave converter at low amplitude signals.

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2(b). Non Linear Wave Shaping-Clampers

Aim: To verify the output of different diode clamping circuits.

Apparatus Required:

Name of the Component/Equipment	Specifications	Quantity
Resistors	10KΩ	1
Capacitor	100uF, 100pF	1
Diode	1N4007	1
Cathode Ray Oscilloscope	20MHz	1
Function generator	1MHz	1
Regulated power supply	0-30V, 1A	1

Theory:

The circuits which are used to add a d.c level as per the requirement to the a.c signals are called clamper circuits. Capacitor, diode, resistor are the three basic elements of a clamper circuit. The clamper circuits are also called d.c restorer or d.c inserter circuits. The clampers are classified as

1. Negative clampers
2. Positive clampers

Circuit Diagrams

Positive peak clamping to 0V:

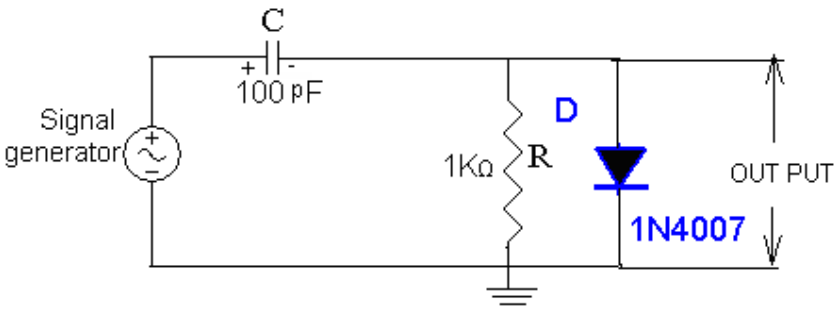


Fig.1

Positive peak clamping to V_r=2v

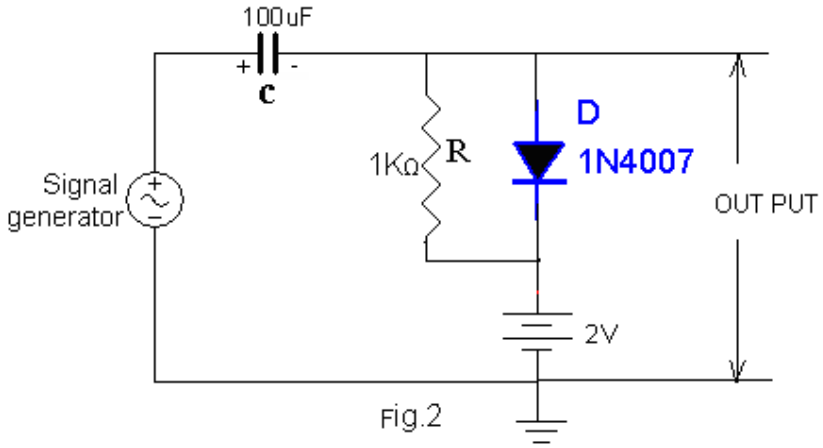


Fig.2

Negative peak clamping to V_r=0v

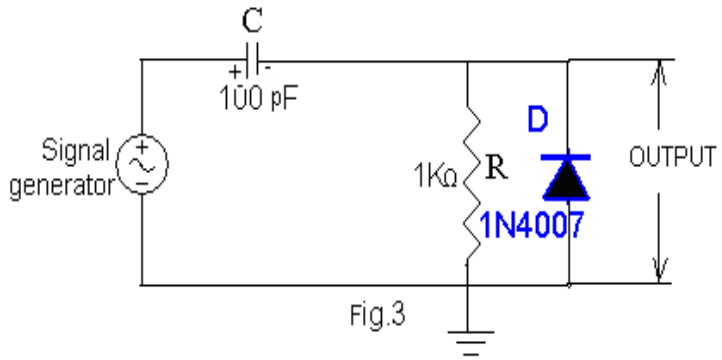


Fig.3

Negative peak clamping to V_r= -2v

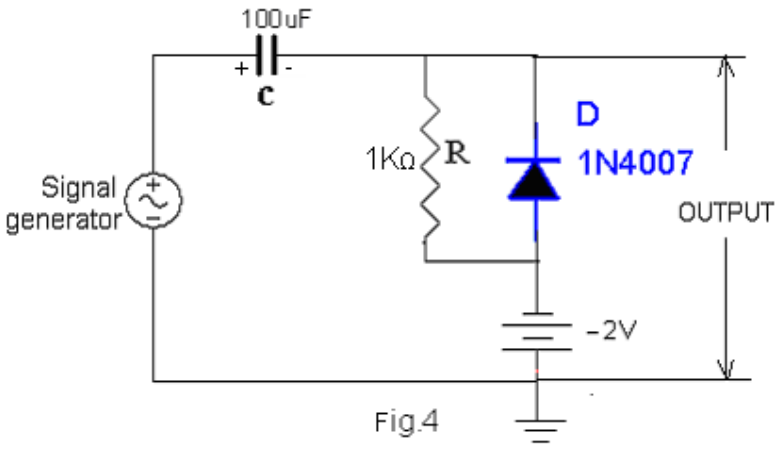


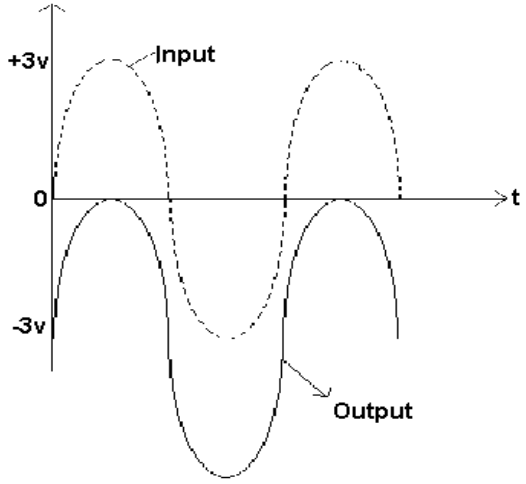
Fig.4

Procedure:

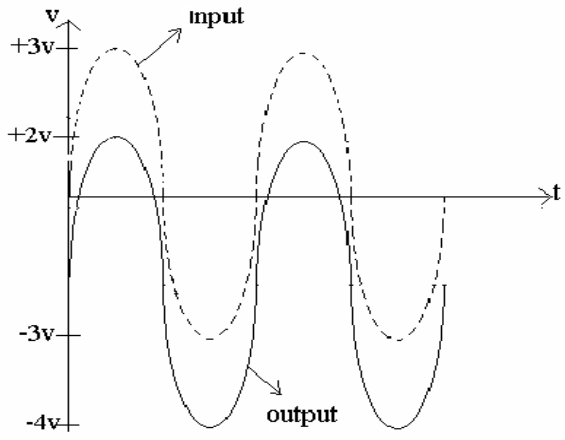
1. Connect the circuit as per circuit diagram Fig 1.
2. Obtain a constant amplitude sine wave from function generator of 6 Vp-p, frequency of 1KHz and give the signal as input to the circuit.
3. Observe and draw the output waveform and note down the amplitude at which clamping occurs.
4. Repeat the steps 1 to 3 for all circuits shown in Fig 2-4.

Model waveforms:

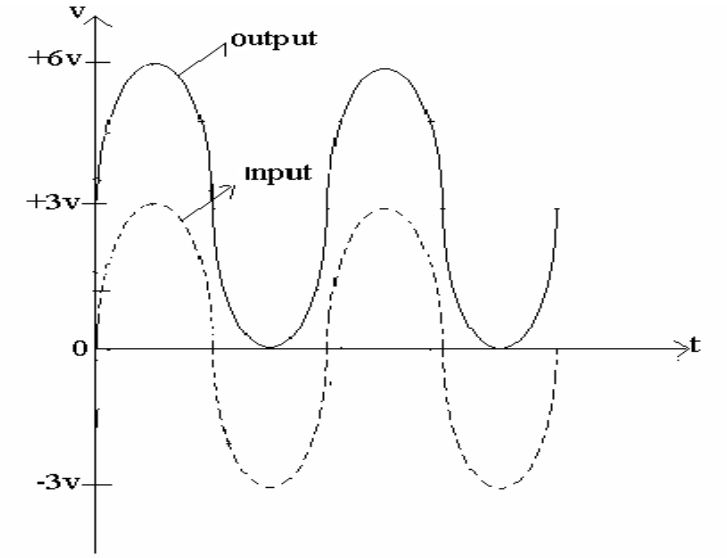
Positive peak clamping to 0V:



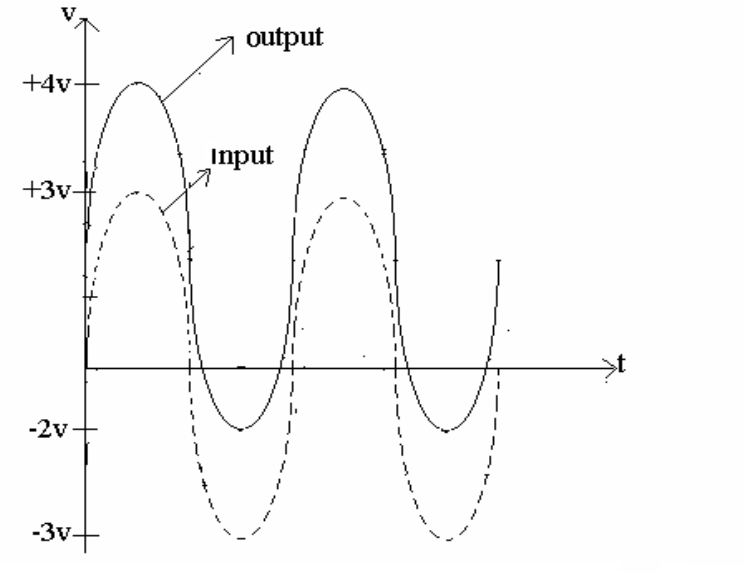
Positive peak clamping to V_r=2V



Negative peak clamping to 0V



Negative peak clamping to Vr= -2V



Precautions:

1. Connections should be made carefully.
2. Verify the circuit before giving supply.
3. Take readings without any parallax error.

Result:

Different clamping circuits are constructed and their performance is observed.

Inference:

In positive peak clamping, Positive peak of the sinusoidal waveform is clamped to 0v when reference voltage is 0v, and clamped to 2v when reference voltage is 2v.That is the waveform is shifted to negative side. So we called this clamper as negative clamper. In negative peak clamping, negative peak of the sinusoidal waveform is clamped to 0v when reference voltage is 0v, and clamped to -2v when reference voltage is -2v.That is the waveform is shifted to positive side. So we called this clamper as positive clamper.

3. Astable Multivibrator using Transistors

Aim: To Observe the ON & OFF states of transistor in an Astable Multivibrator.

Apparatus required:

Name of the Component/Equipment	Specifications	Quantity
Transistor (BC 107)	BC 107	2
Resistors	3.9KΩ, 100KΩ	2
Diode	0A79	1
Capacitor	0.01μF	2
Regulated Power Supply	0-30V, 1A	1
Cathode Ray Oscilloscope	20MHz	1
Function generator	(.1 – 1MHz), 20V $_{p-p}$	1

Theory :

Astable multivibrator : An Astable Multivibrator has two quasi stable states and it keeps on switching between these two states by itself . No external triggering signal is needed. The astable multivibrator cannot remain indefinitely in any one of the two states .The two amplifier stages of an astable multivibrator are regenerative across coupled by capacitors. The astable multivibrator may be to generate a square wave of period, 1.38RC.

Circuit Diagram :

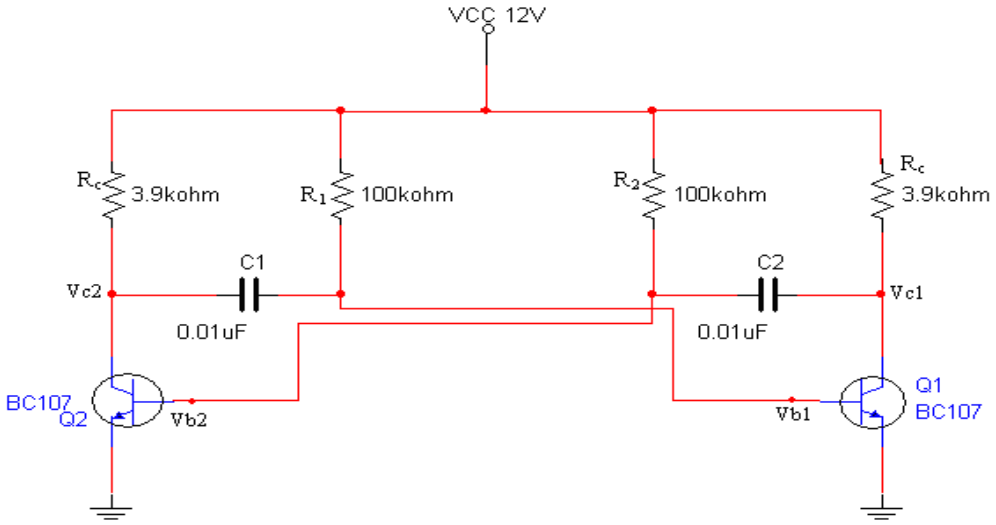


Fig 1 : Astable Multivibrator

Procedure

1. Calculate the theoretical frequency of oscillations of the circuit.
2. Connect the circuit as per the circuit diagram shown in Fig 1.

3. Observe the voltage wave forms at both collectors of two transistors simultaneously.
4. Observe the voltage wave forms at each base simultaneously with corresponding collector voltage as shown in Fig 3.
5. Note down the values of wave forms carefully.
6. Compare the theoratical and practical values.

Calculations:

Theoretical Values:

$RC = R_1C_1 + R_2C_2$

Time Period, $T = 1.368RC$

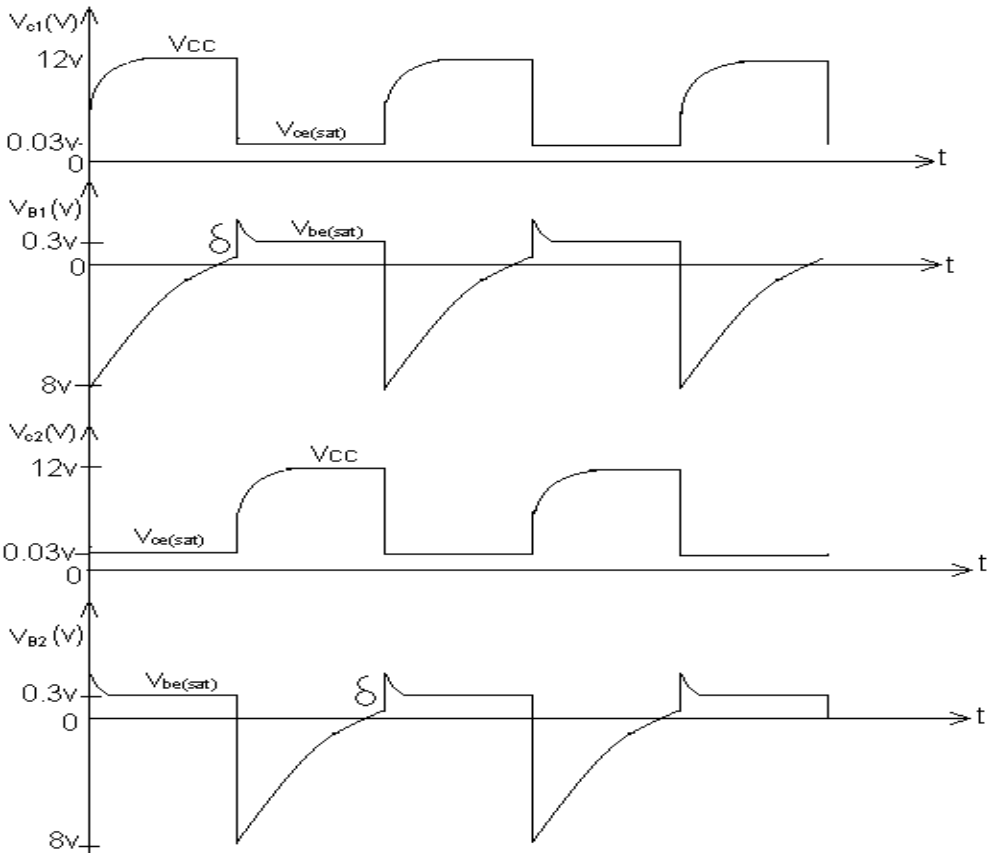
$= 1.368 \times 100 \times 10^{3} \times 0.01 \times 10^{-6}$

$= 93\ \mu$ sec

$= 0.093$ m sec

Frequency, $f = 1/T = 10.75$ kHz

Model waveforms :



Precautions:

1. Connections should be made carefully.
2. Readings should be noted without parallax error.

Result : The wave forms of astable multivibrator has been verified.

4. Monostable Multivibrator using Transistors

Aim:

To observe the stable state and quasi stable state voltages in monostable multivibrator.

Apparatus required:

Name of the Component/Equipment	Specifications	Quantity
Transistor (BC 107)	BC 107	2
Resistors	2.2KΩ	2
	1.5KΩ, 68KΩ, 1KΩ	Each one
Diode	0A79	1
Capacitor	1μF	2
Regulated Power Supply	0-30V, 1A	1
Cathode Ray Oscilloscope	20MHz	1
Function generator	(.1 – 1MHz), 20V $_{p-p}$	1

Theory :

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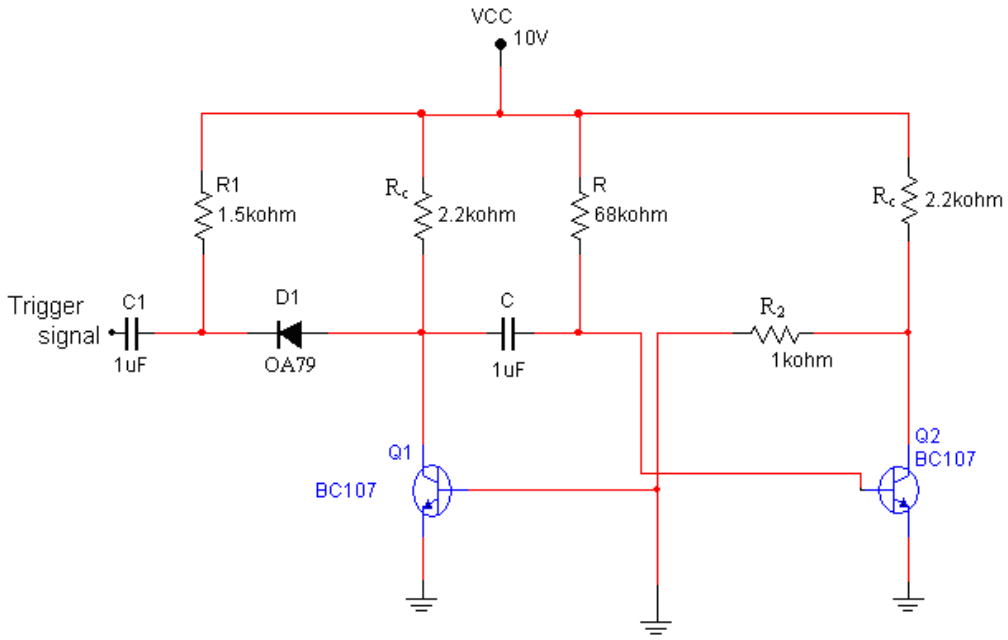
Monostable multivibrator: A monostable multivibrator on the other hand compared to astable, bistable has only one stable state, the other state being quasi stable state. Normally the multivibrator is in stable state and when an externally triggering pulse is applied, it switches from the stable to the quasi stable state. It remains in the quasi stable state for a short duration, but automatically reverse switches back to its original stable state without any triggering pulse. The monostable multivibrator is also referred as ‘one shot’ or ‘uni vibrator’ since only one triggering signal is required to reverse the original stable state. The duration of quasi stable state is termed as delay time (or) pulse width (or) gate time. It is denoted as‘t’.

Circuit Diagram :



Monostable Multivibrator

Procedure :

1. Connect the circuit as per the circuit diagram shown in Fig 2
2. Verify the stable states (Q_1 and Q_2)
3. Apply the square wave of 2Vp-p, 1KHz signal to the trigger circuit.
4. Observe the wave forms at base of each transistor simultaneously.
5. Observe the wave forms at collectors of each transistors simultaneously.
6. Note down the parameters carefully.
7. Note down the time period and compare it with theoretical values.
8. Plot wave forms of V_{b1}, V_{b2},V_{c1} & V_{c2} with respect to time as shown in Fig 4 .

Calculations:

Theoretical Values:

Time Period, T = 0.693RC

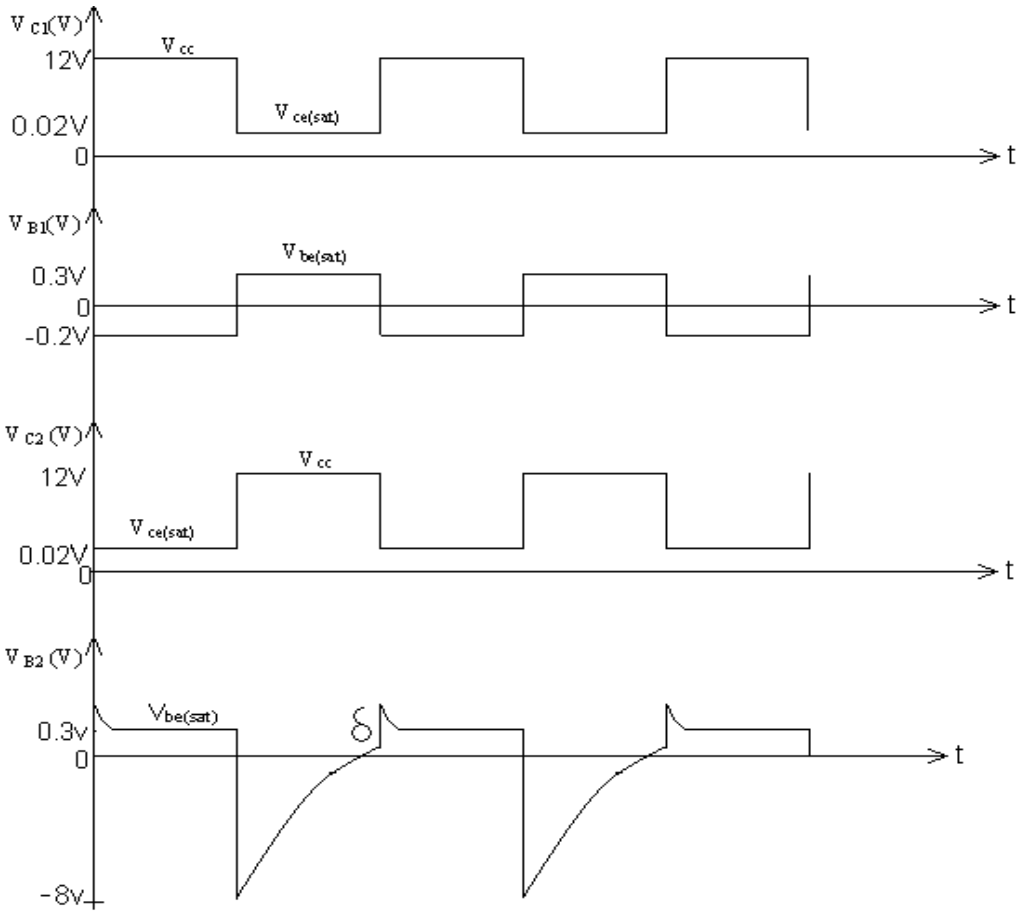
$= 0.693 \times 68 \times 10^{3} \times 0.01 \times 10^{-6}$

= 47μ sec

= 0.047 m sec

Frequency, f = 1/T = 21 kHz

Model waveforms :



Monostable Multivibrator

Precautions:

1. Connections should be made carefully.
2. Readings should be noted without parallax error.

Result :

Stable state and quasi stable state voltages in Monostable multivibrator are observed.

Inference:

.

The output of the monostable multivibrator while it remains in the quasi stable state is a pulse of duration t1 whose value depends up on the circuit components. Hence monostable multivibrator is called as a pulse generator.

5(a). Schmitt Trigger using Transistors

Aim: To generate a square wave from a given sine wave using Schmitt Trigger

Apparatus required:

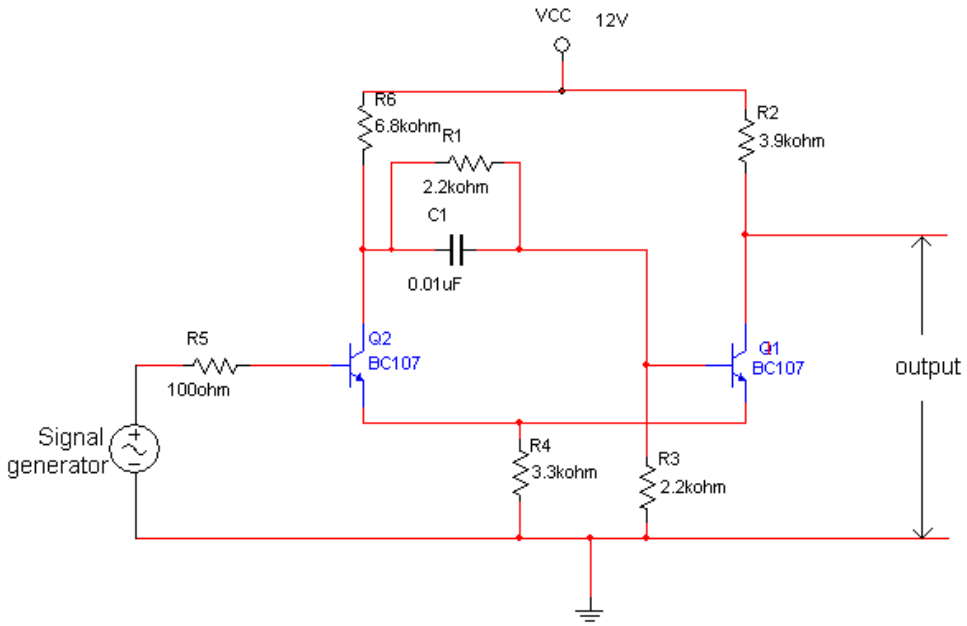
Name of the Component/Equipment	Values/Specifications	Quantity
Transistor	BC 107	2
Resisistors	6.8KΩ,3.9KΩ,2.7KΩ,100Ω	1
	12KΩ	2
	2.2KΩ	3
Capacitor	0.01μF	1
CRO	20MHz	1
Regulated Power Supply	30V	1
Function generator	1MHz	1

Theory:

Schmitt trigger

Schmitt trigger is a Bistable circuit and the existence of only two stable states results form the fact that positive feedback is incorporated into the circuit and from the further fact that the loop gain of the circuit is greater than unity. There are several ways to adjust the loop gain. One way of adjusting the loop gain is by varying Rc1. Under quiescent conditions Q1 is OFF and Q2 is ON because it gets the required base drive from Vcc through Rc1 and R1. So the output voltage is Vo=Vcc-Ic2Rc2 is at its lower level. Until then the output remains at its lower level.

Circuit Diagram:



Schmitt trigger

Procedure:

1 Connect the circuit as per circuit diagram shown in Fig 2.

2 Apply a sine wave of peak to peak amplitude 12V, 1 KHz frequency wave as input to the circuit.

3 Observe input and output waveforms simultaneously in channel 1 and channel 2 of CRO.

4 Note down the input voltage levels at which output changes the voltage level as shown in Fig 3.

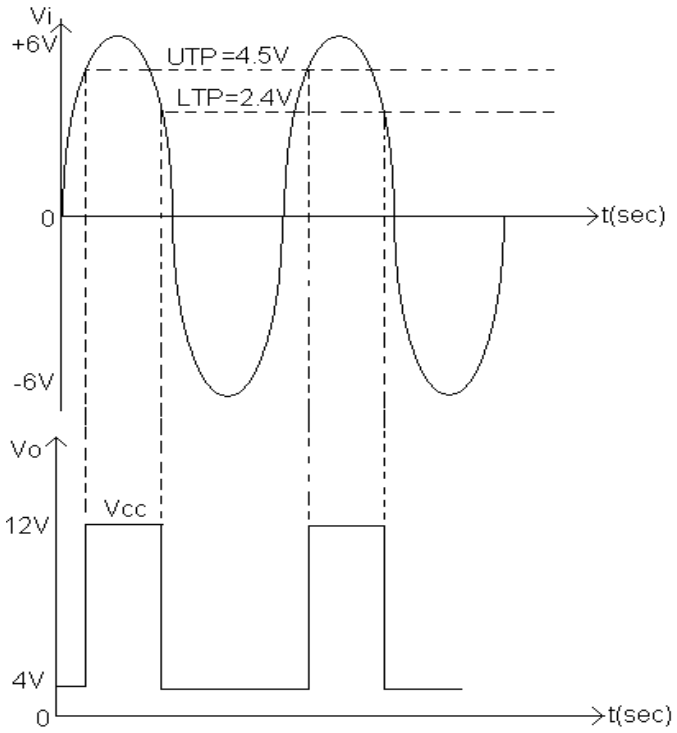
5 Draw the graph between voltage versus time of input and output signals.

Sample Readings:

Schmitt Trigger:

Parameter	Input	Output
Voltage(V_{p-p}),V		
Time period(ms)		

Model Graph



Schmitt trigger

Precautions:

1. Connections should be made carefully.
2. Note down the parameters carefully.
3. The supplied voltage levels should not exceed the maximum rating of the transistor.

Result:

Schmitt trigger circuit is constructed and its performance is observed.

Inference

Schmitt trigger circuit is a emitter coupled bistable circuit, and existence of only two stable states results from the fact that positive feedback is incorporated into the circuit, and from the further fact that the loop gain of the circuit is greater than unity.

5(b). Schmitt Trigger Circuits- using IC 741

Aim: To design the Schmitt trigger circuit using IC 741 .

Apparatus required:

S.No	Equipment/Component name	Specifications/Value	Quantity
1	IC 741	Refer	1
2	Cathode Ray Oscilloscope	(0 – 20MHz)	1
3	Multimeter		1
4	Resistors	100 Ω 56 KΩ	2 1
5	Capacitors	0.1 μf, 0.01 μf	Each one
6	Regulated power supply	(0 -30V),1A	1

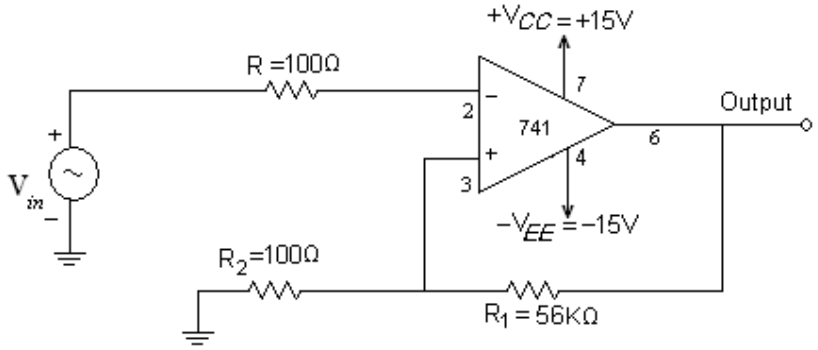
Theory:

The circuit shows an inverting comparator with positive feed back. This circuit converts arbitrary wave forms to a square wave or pulse. The circuit is known as the Schmitt trigger (or) squaring circuit. The input voltage V_{in} changes the state of the output V_o every time it exceeds certain voltage levels called the upper threshold voltage V_{ut} and lower threshold voltage V_{lt}.

When V_o= - V_{sat}, the voltage across R_1 is referred to as lower threshold voltage, V_{lt}. When V_o=+V_{sat}, the voltage across R_1 is referred to as upper threshold voltage V_{ut}.

The comparator with positive feed back is said to exhibit hysterisis, a dead band condition.

Circuit Diagrams:



Schmitt trigger circuit using IC 741

Design:

$V_{utp} = [R_1/(R_1+R_2)](+V_{sat})$

$V_{ltp} = [R_1/(R_1+R_2)](-V_{sat})$

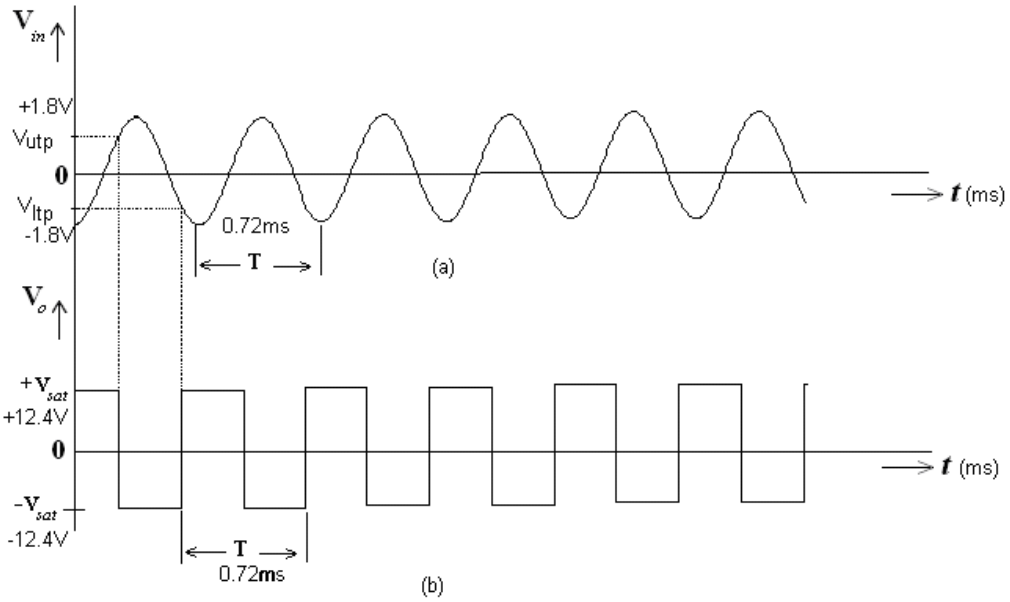
$V_{hy} = V_{utp} - V_{ltp}$

$=[R_1/(R_1+R_2)]\ [+V_{sat} - (-V_{sat})]$

Procedure:

1. Connect the circuit as shown in fig.
2. Apply an arbitrary waveform (sine/triangular) of peak voltage greater than UTP to the input of a Schmitt trigger.
3. Observe the output at pin6 of the IC 741 Schmitt trigger circuit by varying the input and note down the readings as shown in Table 1 and Table 2
4. Find the upper and lower threshold voltages (V_{utp}, V_{Ltp}) from the output wave form.

Wave forms:



Schmitt trigger input wave form

Sample readings:

Table 1:

Parameter	Input		Output	
	741		741	
Voltage(V_{p-p})				
Time period(ms)				

Table 2:

Parameter	741
V_{utp}	
V_{ltp}	

Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Results:

UTP and LTP of the Schmitt trigger are obtained by using IC 741 as shown in Table 2.

Inferences: Schmitt trigger produces square waveform from a given signal.

Experiment no: 6 Measurement of op-Amp parameters

Aim: To measure the op-Amp parameters such as

(a) Input Bias Current

(b) Input Offset current

(c) Input offset voltage of given op-Amp

(d) SlewRate

Apparatus:

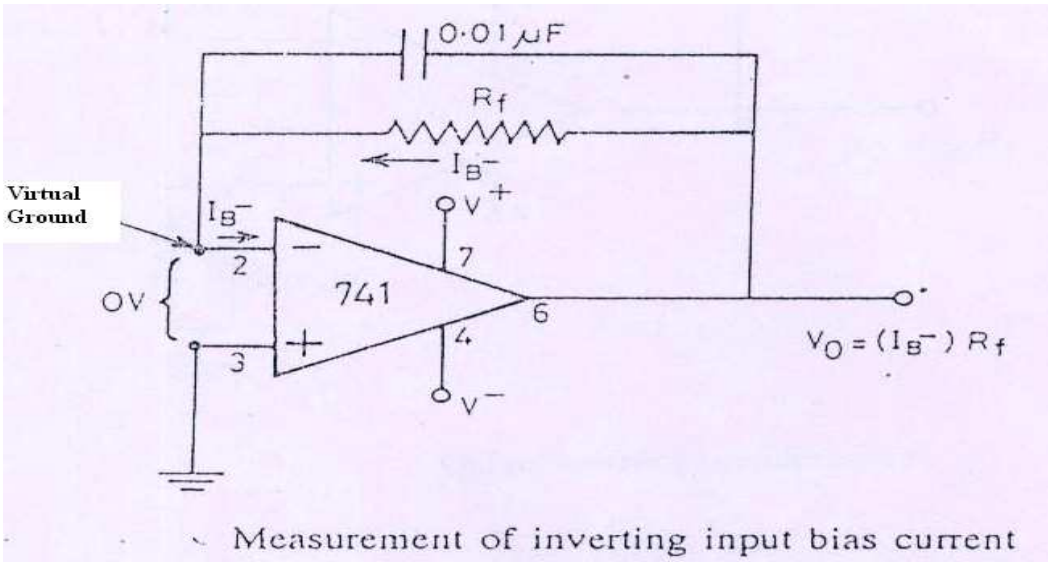
- 741 Op-Amps
- Sine wave Signal generator
- Resistors, capacitors
- 10KΩ, 100Ω, 1MΩ, 0.01uF

Procedure:

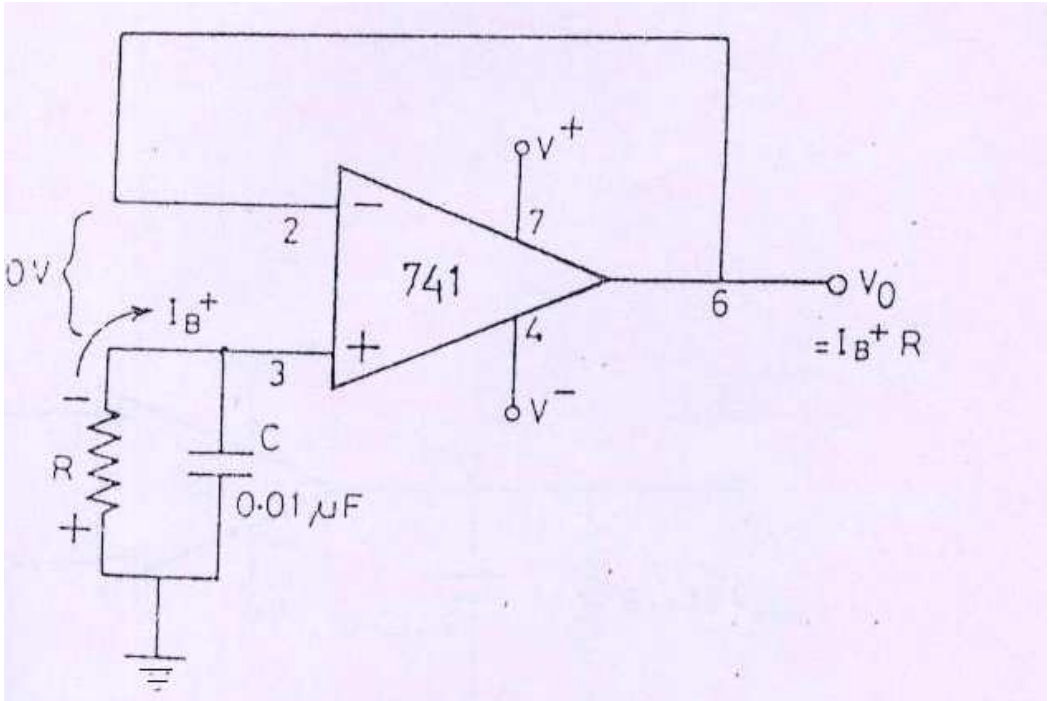
1. Set up the circuit shown in fig 1.1 to measure I_B^-.
2. Set up the circuit shown in fig 1.2 to measure I_B^+.
3. Select the large resistor (in MΩ) and measure the out put voltage.
4. Calculate $I_b = \frac{V_0}{R_f}, I_b^+ = \frac{V_0}{R}$
5. Calculate $I_B = \frac{I_B^+ + I_B^-}{2}$
6. Set up the circuit Ckt shown in fig 1.3 to measure offset current loss. I_{os} = Vo/Rf.
7. Set up the circuit shown in fig 1.4 $V_0 = (1+R_f/R_i)\, V_{OS} + I_{OS} R_f = (1+ R_f/R_i)\, V_{os}$
8. Set up the ckt shown in fig 1.5
9. Adjust the input sine-wave signal generator so that the output is 1V peak sine wave at I KHz.
10. Slowly increase the input signal frequency until the output gets just distorted.
11. Calculate slew rate, $SR=2\pi f V_m/10^6$ V/μS where V_m=peak output amplitude in volts and f= frequency in Hz.
12. Now give a square-wave input and repeat step-9 increase the i/p frequency slowly until the output is just barely a triangular wave. The SR= AVo/At V/jis where V_0 is the change in the output voltage amplitude in volts, At = time required for AVo in j.is.

Precautios:

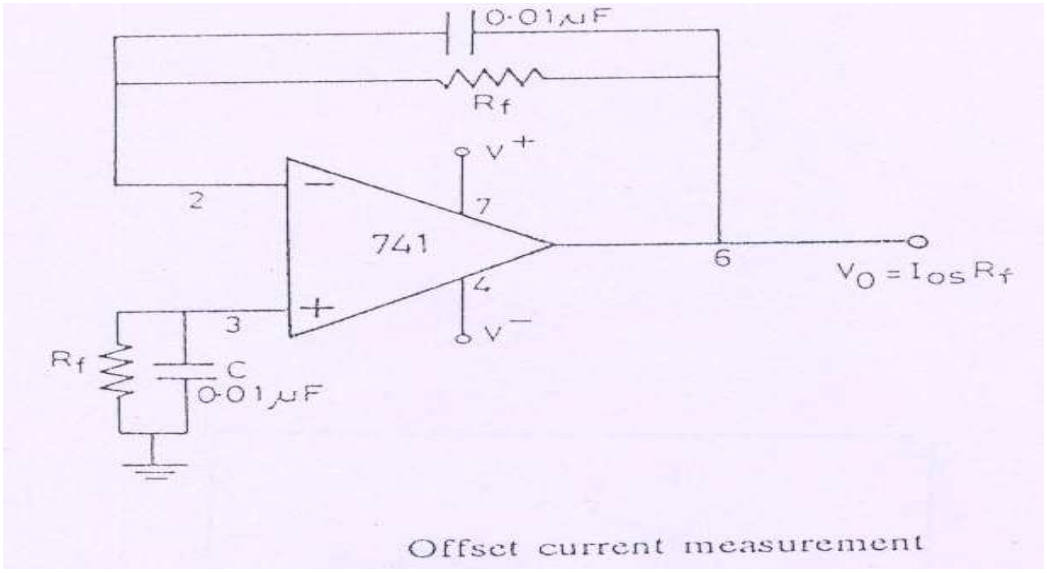
1. Don't disturb the set up while performing experiment.
2. Take the readings with out parallax error



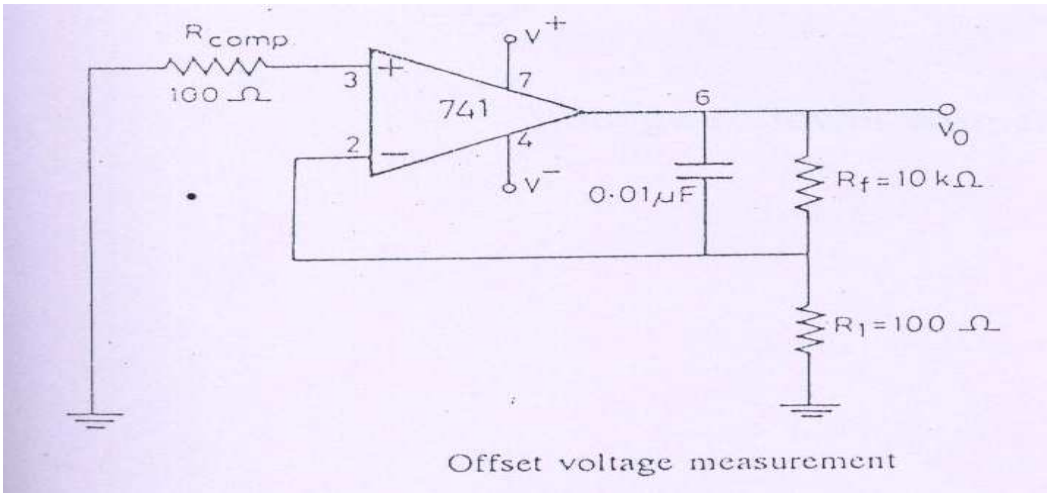
Measurement of inverting input bias current



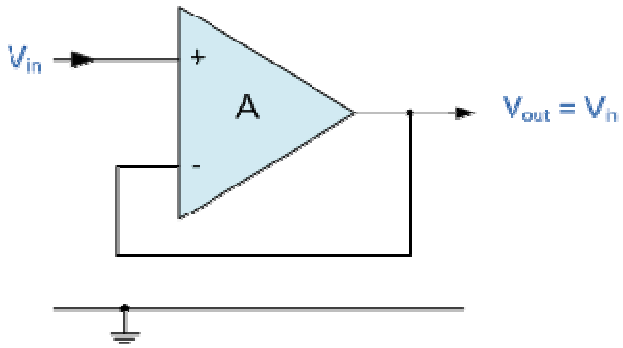
. Measurement of non-inverting input bias current



Offset current measurement



Offset voltage measurement



7. Applications of Op-Amp

Aim: To design adder for the given signals by using operational amplifier and to design integrator and differentiator for a given input (square/sine)

Apparatus required:

S.No	Equipment/Component name	Specifications/Value	Quantity
1	IC 741	Refer Appendix A	1
2	Capacitors	0.1μf, 0.01μf	Each one
3	Resistors	159Ω, 1.5kΩ	Each one
4	Resistor	1kΩ	4
5	Diode	0A79	2
6	Regulated Power Supply	(0 – 30V),1A	2
7	Function Generator	(.1 – 1MHz), 20V $_{p-p}$	1
8	Cathode Ray Oscilloscope	(0 – 20MHz)	1
9	Multimeter	3 ^{½} digit display	1

Theory

Adder*:* A two input summing amplifier may be constructed using the inverting mode. The adder can be obtained by using either non-inverting mode or differential amplifier. Here the inverting mode is used. So the inputs are applied through resistors to the inverting terminal and non-inverting terminal is grounded. This is called “virtual ground”, i.e. the voltage at that terminal is zero. The gain of this summing amplifier is 1, any scale factor can be used for the inputs by selecting proper external resistors.

Integrator: In an integrator circuit, the output voltage is the integration of the input voltage.

The output voltage of an integrator is given by $V_o = -1/R_1C_f \int_o^t Vidt$

At low frequencies the gain becomes infinite, so the capacitor is fully charged and behaves like an open circuit. The gain of an integrator at low frequency can be limited by connecting a resistor in shunt with capacitor

Differentiator: In the differentiator circuit the output voltage is the differentiation of the input voltage. The output voltage of a differentiator is given by $V_o = -RfC_1 \frac{dV_{in}}{df}$.The input impedance of this circuit decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise. At high frequencies circuit may become unstable.

For pin configuration and specifications of opamp (IC 741), refer Appendix-B

Circuit Diagrams:

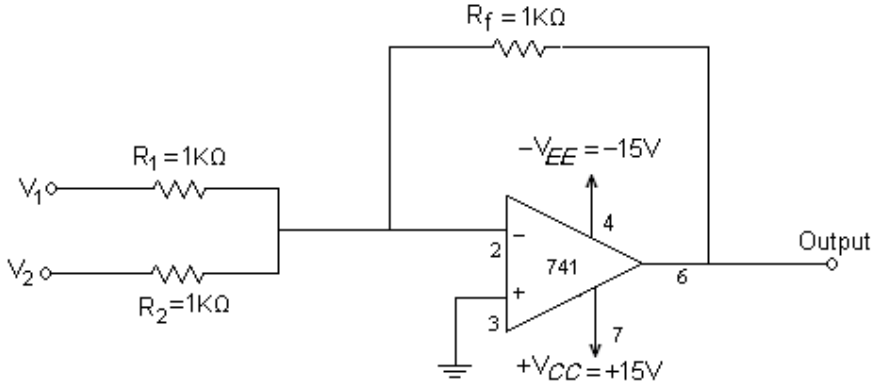


Fig1: Adder

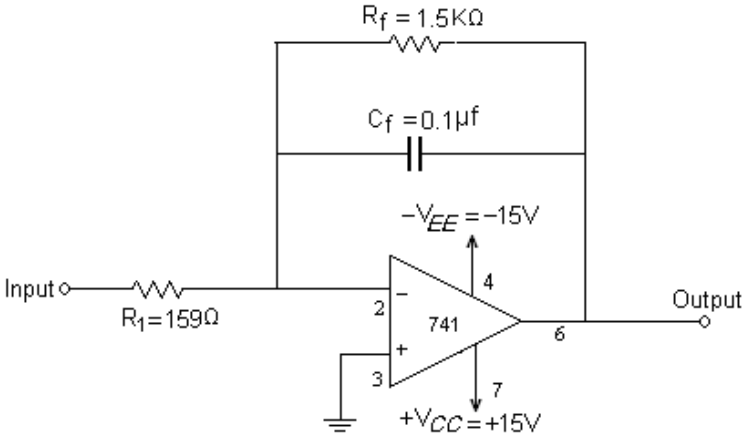


Fig 2: Integrator

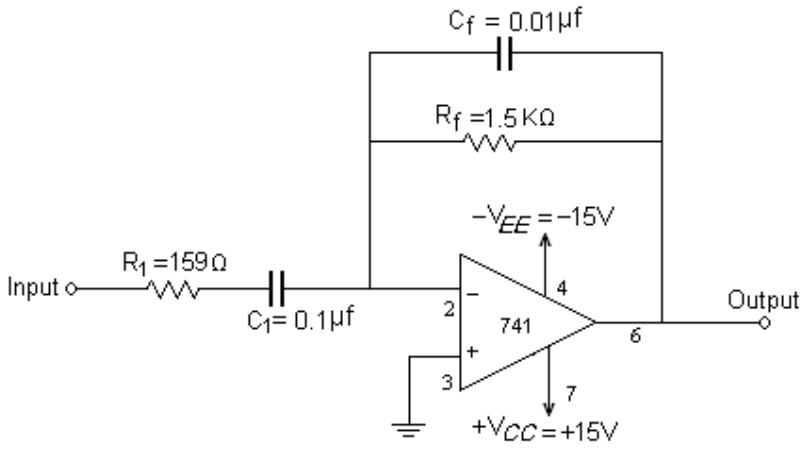


Fig 3: Differentiator

Design equations:

Adder:

Output voltage, $V_o = -(V_1+V_2)$

Integrator:

Choose $T = 2\pi R_f C_f$

Where T= Time period of the input signal

Assume C_f and find R_f

Select $R_f = 10R_1$

$$V_{o\,(p\text{-}p)} = \frac{-1}{R_1 C_f}\int_o^{T/2} V_{i(p-p)}\,dt$$

Differentiator

Select given frequency $f_a = 1/(2\pi R_f C_1)$, Assume C_1 and find R_f

Select $f_b = 10\ f_a = 1/2\pi R_1 C_1$ and find R_1

From $R_1C_1 = R_fC_f$, find C_f

Procedure:

Adder:

1. Connect the circuit as per the diagram shown in fig 1.
2. Apply the supply voltages of ±15V to pin7 and pin4 of IC741 respectively.
3. Apply the inputs V_1 and V_2 as shown in fig 1.
4. Apply two different signals (DC/AC) to the inputs
5. Vary the input voltages and note down the corresponding output at pin 6 of the IC 741 adder circuit.
6. Notice that the output is equal to the sum of the two inputs.

Integrator

1 Connect the circuit as per the diagram shown in fig 2

2 Apply a square wave/sine input of 4V(p-p) of 1KHz

3 Observe the o/p at pin 6.

4 Draw input and output waveforms as shown in fig: 4

Differentiator

1. Connect the circuit as per the diagram shown in fig 3
2. Apply a square wave/sine input of 4V(p-p) of 1KHz
3. Observe the output at pin 6
4. Draw the input and output waveforms as shown in fig: 5

Wave Forms:

Integrator

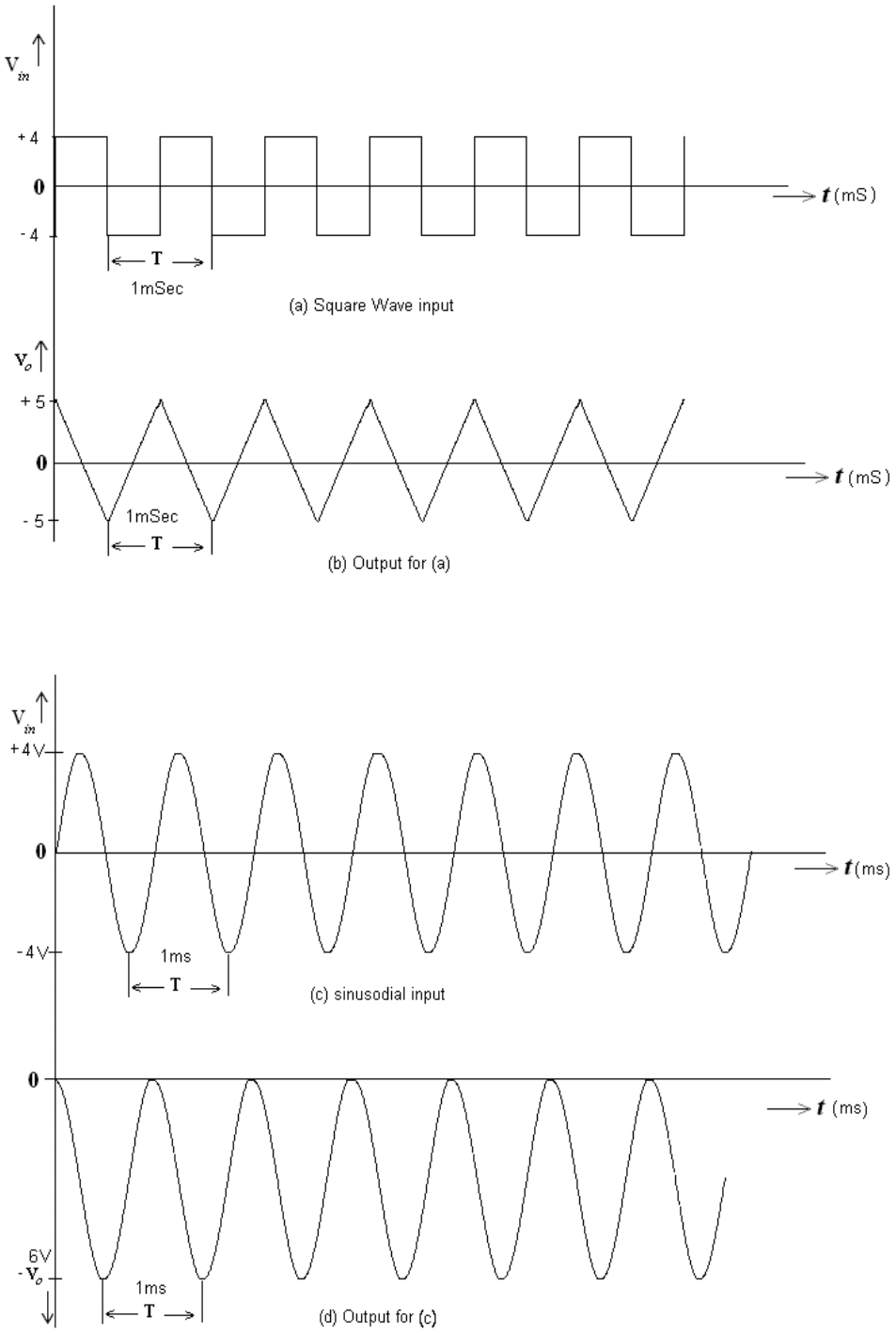


Fig 4: Input and output waves forms of integrator

Differentiator

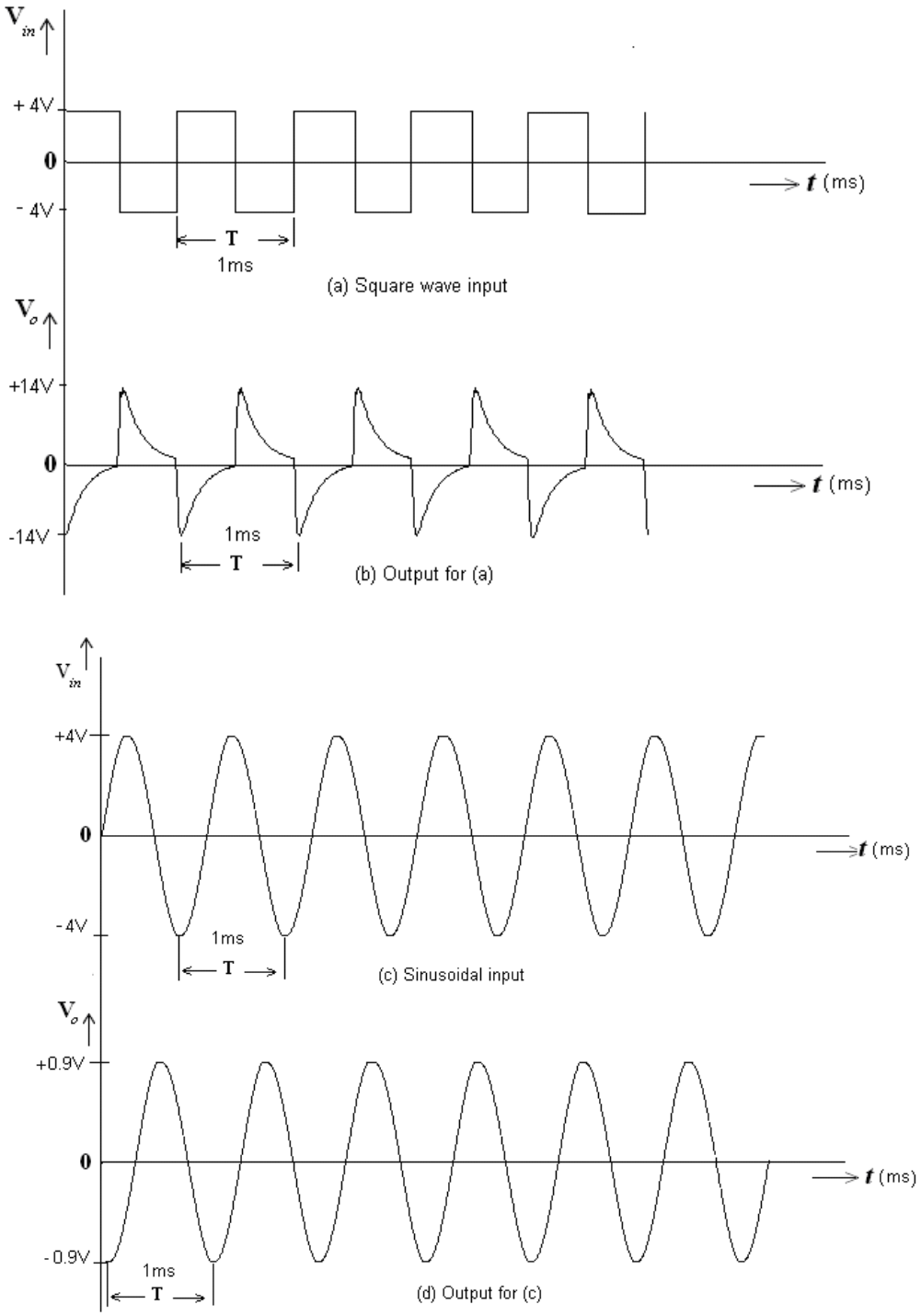


Fig 5 :Input and output waveforms of Differentiator

Sample readings:

Adder:

i/p_1(V)	i/p_2(V)	V_o(V)

Integrator

Input –Square wave		Output - Triangular	
Amplitude(V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)

Input –sine wave		Output - cosine	
Amplitude(V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)

Differentiator

Input –square wave		Output - Spikes	
Amplitude (V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)

Input –sine wave		Output - cosine	
Amplitude (V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)

Model Calculations:

Adder

$V_o = - (i/p_1 + i/p_2)$

If i/p_1 = 2.5V and i/p_2 = 2.5V, then

V_o = - (2.5+2.5) = -5V.

Integrator:

For T= 1 msec

f_a= 1/T = 1 KHz

f_a = 1 KHz = $1/(2\pi R_f C_f)$

Assuming Cf= 0.1μf, R_f is found from $R_f=1/(2\pi f_a C_f)$

R_f=1.59 KΩ

$R_f = 10\ R_1$

R_1= 159Ω

Differentiator

For T = 1 msec

f= 1/T = 1 KHz

f_a = 1 KHz = $1/(2\pi R_f C_1)$

Assuming C_1= 0.1μf, R_f is found from $R_f=1/(2\pi f_a C_1)$

R_f=1.59 KΩ

$f_b = 10\ f_a = 1/2\pi R_1 C_1$

for C_1= 0.1μf;

R_1 =159Ω

Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Result: For a given square wave and sine wave, output waveforms for integrator and differentiator are observed and the adder circuit is designed.

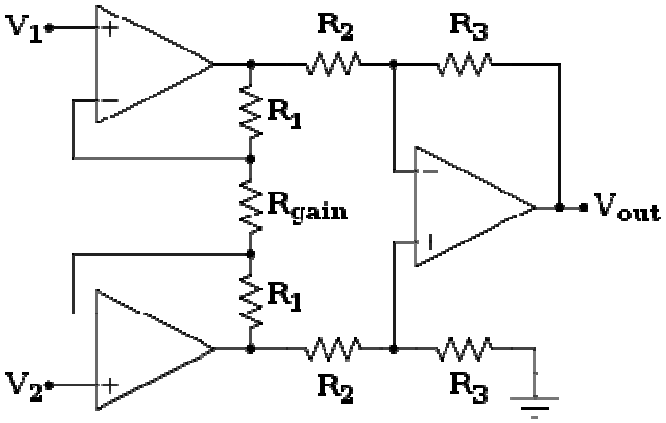
Inferences: Spikes and triangular waveforms can be obtained from a given square waveform by using differentiator and integrator respectively and the given signals can be added by using the adder circuit.

Experiment no: *8* Instrumentation Amplifier using op-Amp

AIM: To study the operation of instrumentation Amplifier

Apparatus:

- µ.A 741 op-Amps
- Resistors of 1KΩ, 4.7KΩ, 10KΩ



Procedure:

1. Set up the circuit shown in fig 2-

Calculate the output voltage "V_{out}"

3. Calculate the V_{out} where $V_{out} = (V_2-V_1)\,(1+2R_1/R_{gain})\,(R_3/R_2)$
4. Compare it with practical output voltage.
5.
6.
7. **Important features of Instrumentation amplifier:**

- High gain accuracy
- High CMRR
- High gain stability with low-temperature Co-efficient
- Low dc-offset
- Low output impedance

Applications:

Measurement & control of temperature, humidity light intensity, waler flow .. .etc.

Precautions:

1. Loose connections should he avoided
2. Positive and Negative supplies should be given correctly to IC 741
3. Waveforms should be taken in accordance with the scale.

9. WAVEFORM GENERATION USING OP-AMP (SQUARE & TRIANGULAR)

Aim: To generate square wave and Triangular wave form by using OPAMPs.

Apparatus required:

S.No	Equipment/Component name	Specifications/Value	Quantity
1	741 IC	Refer Appendix A	2
2	Capacitors	0.01μf,0.001μf	Each one
3	Resistors Resistors	86kΩ ,68kΩ ,680kΩ 100kΩ	Each one 2
4	Regulated Power supply	(0 – 30V),1A	1
5	Cathode Ray Oscilloscope	(0 -20MHz)	1

Theory: Function generator generates waveforms such as sine, triangular, square waves and so on of different frequencies and amplitudes. The circuit shown in Fig1 is a simple circuit which generates square waves and triangular waves simultaneously. Here the first section is a square wave generator and second section is an integrator. When square wave is given as input to integrator it produces triangular wave.

Circuit Diagram:

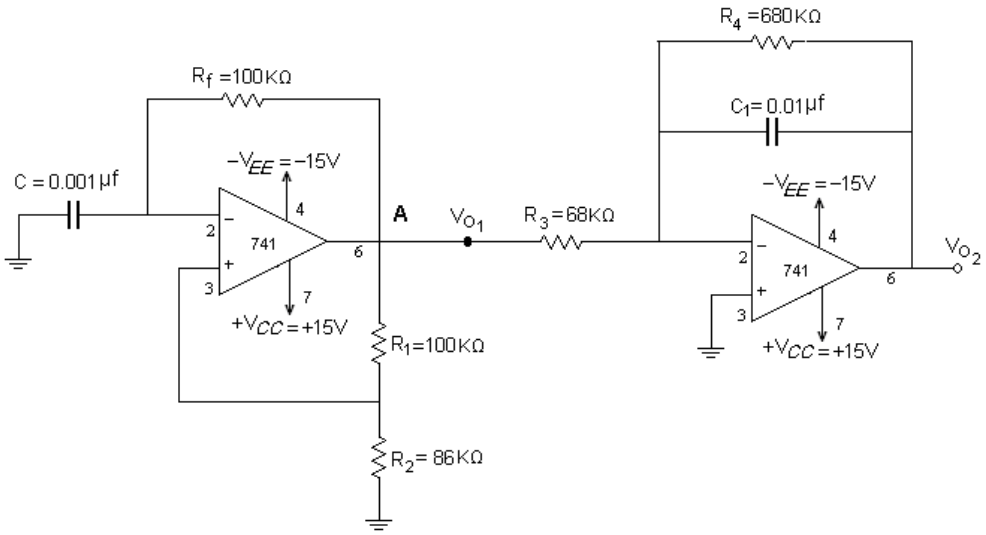


Fig1 Function Generator

Design:

Square wave Generator:

$T = 2R_fC \ln (2R_2 + R_1/ R_1)$

Assume $R_1 = 1.16\ R_2$

Then $T = 2R_fC$

Assume C and find R_f

Assume R_1 and find R_2

Integrator:

Take $R_3 C_f >> T$

$R_3 C_f = 10T$

Assume C_f find R_3

Take $R_3C_f = 10T$

Assume $C_f = 0.01\mu f$

$R_3 = 10T/C$

$= 20K\Omega$

Procedure:

1. Connect the circuit as per the circuit diagram shown in Fig 1.
2. Obtain square wave at A and Triangular wave at V_o as shown in fig (a) and (b).
3. Draw the output waveforms as shown in fig (a) and (b).

Model Calculations:

For T= 2 m sec

$T = 2 R_fC$

Assuming C= 0.1μf

$R_f = 2.10^{-3}/ 2.01.10^{-6}$

$= 10 K\Omega$

Assuming $R_1 = 100$ K

$R_2 = 86 K\Omega$

Sample readings:

Square Wave:

$V_{p-p} = 26$ V(p-p)

T = 1.8 msec

Triangular Wave:

$V_{p-p} = 1.3$ V

T= 1.8 msec

Wave Forms:

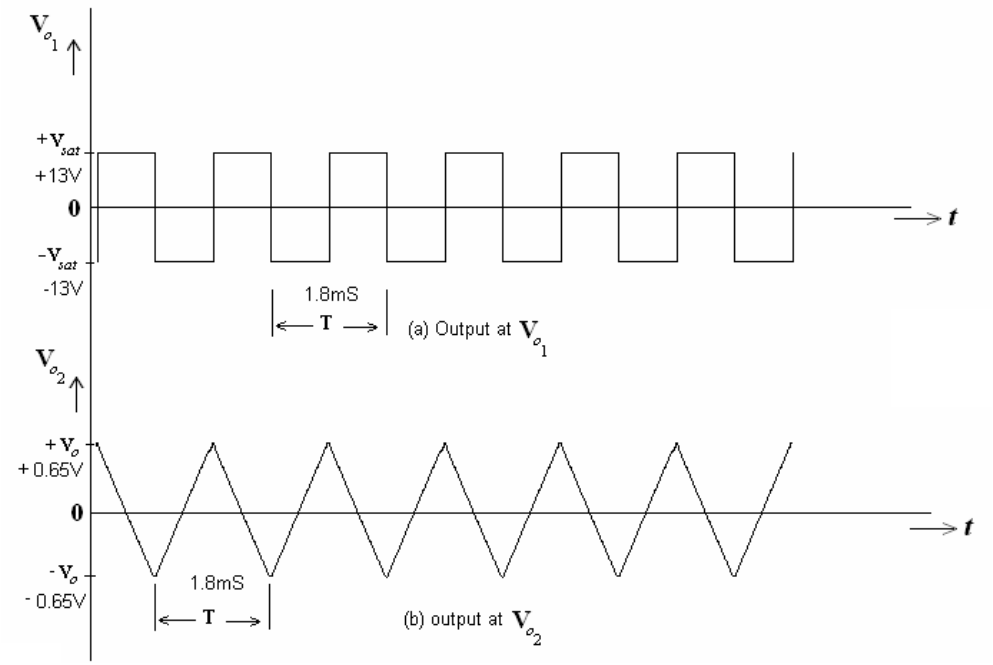


Fig (a): Output at 'A'

Fig (b): Output

Precautions: Check the connections before giving the power supply.

Readings should be taken carefully.

Result: Square wave and triangular wave are generated and the output waveforms are observed.

Inferences: Various waveforms can be generated.

10. Design Of Active Filters – Lpf, Hpf (First Order)

Aim: To design and obtain the frequency response of

i) First order Low Pass Filter (LPF)

ii) First order High Pass Filter (HPF)

Apparatus required:

S.No	Equipment/Component name	Specifications/Value	Quantity
1	IC 741	Refer Appendix A	1
2	Resistors Variable Resistor	10k ohm 20kΩ pot	3 1
3	capacitors	0.01μf	1
4	Cathode Ray Oscilloscope	(0 – 20MHz)	1
5	RPS	(0 – 30V),1A	1
6	Function Generator	(1Hz – 1MHz)	1

Theory:

a) LPF:

A LPF allows frequencies from 0 to higher cut of frequency, f_H. At f_H the gain is 0.707 A_{max}, and after f_H gain decreases at a constant rate with an increase in frequency. The gain decreases 20dB each time the frequency is increased by 10. Hence the rate at which the gain rolls off after f_H is 20dB/decade or 6 dB/ octave, where octave signifies a two fold increase in frequency. The frequency $f=f_H$ is called the cut off frequency because the gain of the filter at this frequency is down by 3 dB from 0 Hz. Other equivalent terms for cut-off frequency are -3dB frequency, break frequency, or corner frequency.

b) HPF:

The frequency at which the magnitude of the gain is 0.707 times the maximum value of gain is called “low cut off frequency”. Obviously, all frequencies higher than f_L are pass band frequencies with the highest frequency determined by the closed –loop band width all of the op-amp.

Circuit diagrams:

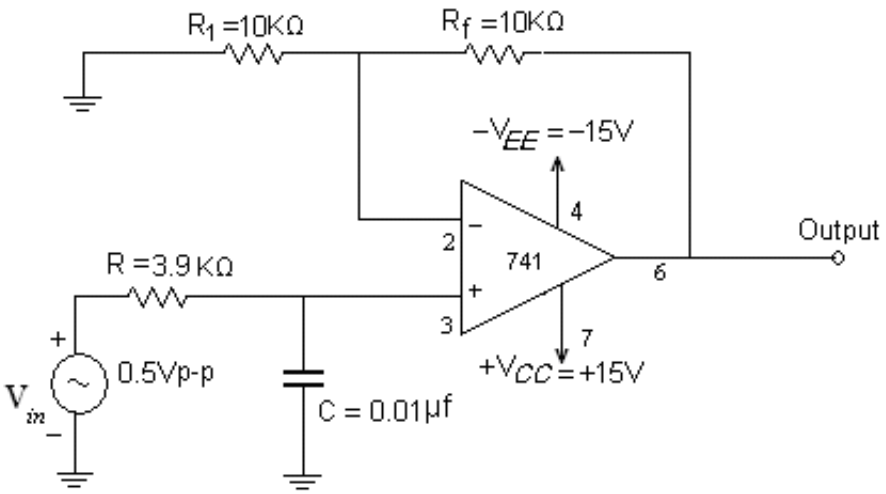


Fig 1: Low pass filter

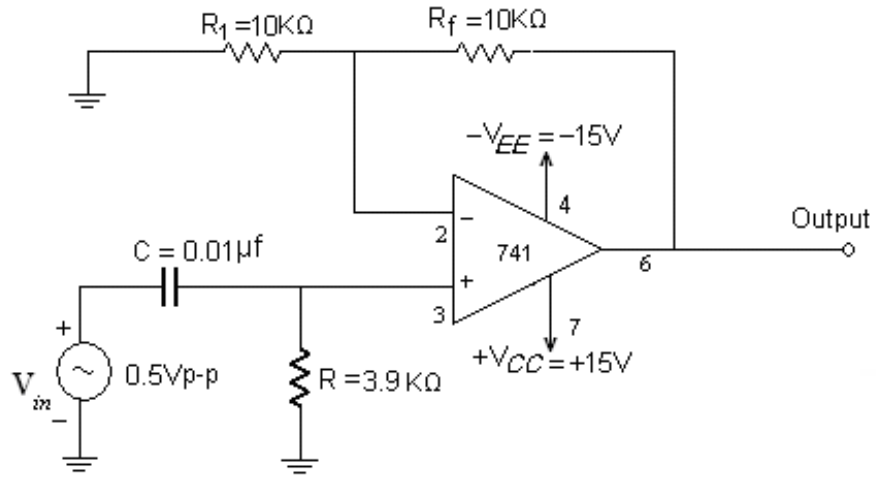


Fig 2: High pass filter

Design:

First Order LPF: To design a Low Pass Filter for higher cut off frequency f_H = 4 KHz and pass band gain of 2

$f_H = 1/(2\pi RC)$

Assuming C=0.01 µF,the value of R is found from

$R = 1/(2\pi f_H C)\ \Omega = 3.97K\Omega$

The pass band gain of LPF is given by $A_F = 1 + (R_F/R_1) = 2$

Assuming R_1=10 KΩ, the value of R_F is found from

$R_F = (A_F - 1)\ R_1 = 10K\Omega$

First Order HPF: To design a High Pass Filter for lower cut off frequency f_L = 4 KHz and pass band gain of 2

$f_L = 1/(2\pi RC)$

Assuming C=0.01 µF,the value of R is found from

$R = 1/(2\pi f_L C)\ \Omega = 3.97K\Omega$

The pass band gain of HPF is given by $A_F = 1 + (R_F/R_1) = 2$

Assuming R_1=10 KΩ, the value of R_F is found from

$R_F = (A_F - 1)\ R_1 = 10K\Omega$

Procedure:

First Order LPF

1. Connections are made as per the circuit diagram shown in fig 1.
2. Apply sinusoidal wave of constant amplitude as the input such that op-amp does not go into saturation.
3. Vary the input frequency and note down the output amplitude at each step as shown in Table (a).
4. Plot the frequency response as shown in fig 3 .

First Order HPF

1. Connections are made as per the circuit diagrams shown in fig 2.
2. Apply sinusoidal wave of constant amplitude as the input such that op-amp does not go into saturation.
3. Vary the input frequency and note down the output amplitude at each step as shown in Table (b).
4. Plot the frequency response as shown in fig 4.

Tabular Form and Sampled Values:

a)LPF b) HPF

Input voltage V_{in} = 0.5V

Frequency	O/P Voltage(V)	Voltage Gain Vo/Vi	Gain indB

Frequency	O/P Voltage(V)	Voltage Gain Vo/Vi	Gain indB

Model graphs :

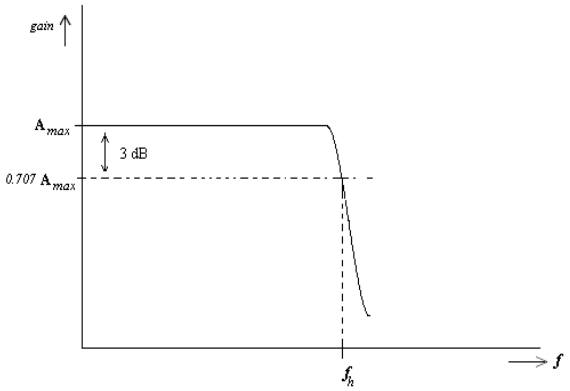
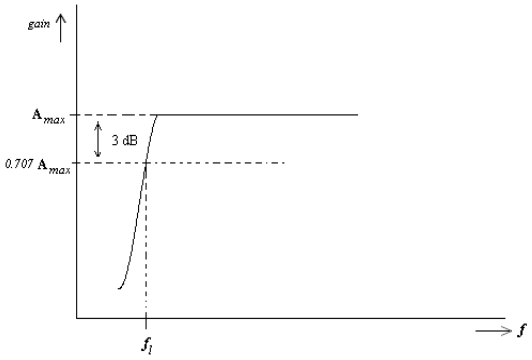


Fig (3)

Frequency response characteristics of LPF



Fig(4)

Frequency response characteristics of HPF

Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Precautions: V_{CC} and V_{EE} must be given to the corresponding pins.

Result: First order low-pass filter and high-pass filter are designed and frequency response characteristics are obtained.

Inferences: By interchanging R and C in a low-pass filter, a high-pass filter can be obtained.

11. APPLICATIONS OF IC 555 TIMERS

(Monostable &Astable multivibrators)

Aim: To generate a pulse using monostable multivibrator and to generate unsymmetrical square and symmetrical square waveforms using IC555

Apparatus required:

S.No	Equipment/Component name	Specifications/Value	Quantity
1	IC 555	Refer Appendix B	1
2	Resistors	3.6kΩ,7.2kΩ	Each one
3	Resistors	10kΩ	2
4	Capacitors	0.1μf,0.01μf	Each one
5	Diode	OA79	1
6	Regulated Power supply	(0 – 30V),1A	1
7	Cathode Ray Oscilloscope	(0 – 20MHz)	1

Theory:

Monostable operation:

A Monostable Multivibrator, often called a one-shot Multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or stand by mode the output of the circuit is approximately Zero or at logic-low level. When an external trigger pulse is obtained, the output is forced to go high ($\cong V_{CC}$). The time the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The Monostable circuit has only one stable state (output low), hence the name monostable. Normally the output of the Monostable Multivibrator is low.

When the power supply V_{CC} is connected, the external timing capacitor 'C" charges towards V_{CC} with a time constant (R_A+R_B) C. During this time, pin 3 is high ($\approx V_{CC}$) as Reset R=0, Set S=1 and this combination makes $\overline{Q}$=0 which has unclamped the timing capacitor 'C'. For pin configuration and specifications, see Appendix-C

Astable operation:

When the capacitor voltage equals 2/3 V_{CC}, the UC triggers the control flip flop on that $\overline{Q}$=1. It makes Q1 ON and capacitor 'C' starts discharging towards ground through R_B and transistor Q1 with a time constant R_BC. Current also flows into Q1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q1.

The minimum value of R_A is approximately equal to $V_{CC}/0.2$ where 0.2A is the maximum current through the ON transistor Q1.

During the discharge of the timing capacitor C, as it reaches $V_{CC}/3$, the LC is triggered and at this stage S=1, R=0 which turns $\overline{Q}$=0. Now $\overline{Q}$=0 unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between 2/3 V_{CC} and 1/3 V_{CC} respectively. The length of time that the output remains HIGH is the time for the capacitor to charge from 1/3 V_{CC} to 2/3 V_{CC}.

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{CC} volts is given by $V_C = V_{CC} (1- e^{-t/RC})$

Total time period $T = 0.69 (R_A + 2 R_B) C$

$f= 1/T = 1.44/ (R_A + 2R_B) C$

Circuit Diagrams:

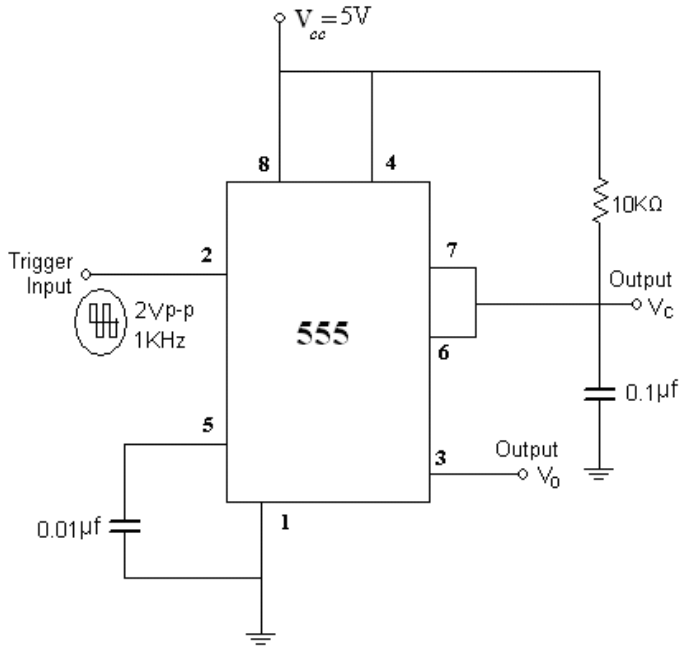


Fig 1: Monostable operation

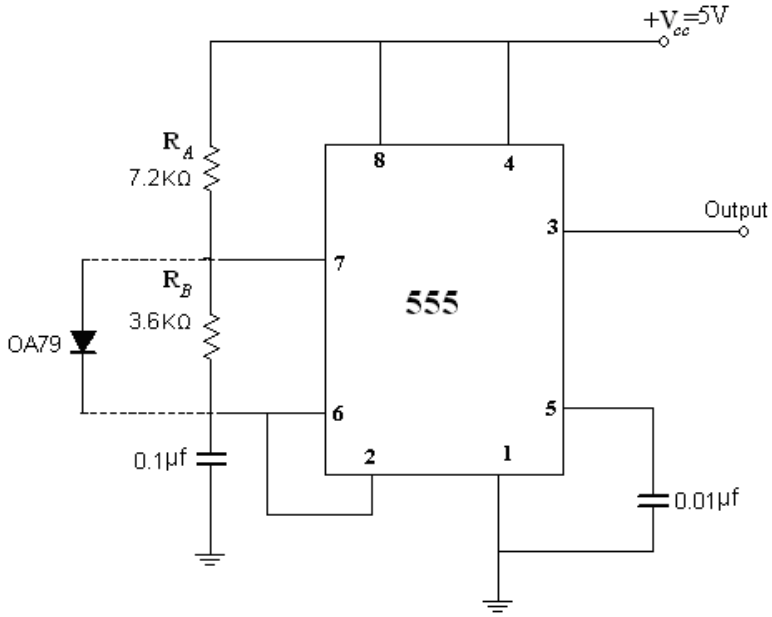


Fig 2: Astable operation

Design:

Monostable operation:

Consider V_{CC} = 5V, for given t_p

Output pulse width $t_p = 1.1\ R_A\ C$

Assume C in the order of microfarads & Find R_A

Astable operation:

Formulae: $f = 1/T = 1.44/ (R_A+2R_B)\ C$

Duty cycle, $D = t_c/T = R_A + R_B/(R_A+2R_B)$

Model calculations:

Monostable operation:

If C=0.1 μF , R_A = 10k then t_p = 1.1 mSec

Trigger Voltage =4 V

Astable operation:

Given f=1 KHz and c=0.1μF, D=0.25

$\therefore 1\ KHz = 1.44/ (RA+2R_B) \times 0.1 \times 10^{-6}$ and $0.25 = R_A+R_B/ R_A+2R_B$

Solving both the above equations, we obtain R_A & R_B as

R_A = 7.2K Ω

R_B = 3.6K Ω

Procedure:

Monostable operation:

1. Connect the circuit as shown in the circuit diagram as shown in Fig 1.
2. Apply Negative triggering pulses at pin 2 of frequency 1 KHz as shown in Fig 3(a).
3. Observe the output waveform and capacitor voltage as shown in Fig 3 (b)and (c) and measure the pulse duration
4. Theoretically calculate the pulse duration as T_{high}=1.1. R_aC
5. Compare it with experimental values.

Astable operation:

I) Unsymmetrical Square wave

1. Connect the circuit as per the circuit diagram shown in Fig 2 without connecting the diode OA 79.
2. Observe and note down the output waveform at pin 3 and across timing capacitor as shown in Fig 4(a) and (b).
3. Measure the frequency of oscillations and duty cycle and then compare with the given values.
4. Sketch both the waveforms to the same time scale.

II) Symmetrical square waveform generator:

1. Connect the diode OA79 as shown in fig (ii) to get D=0.5 or 50%.
2. Choose R_a=R_b = 10KΩ and C=0.1μF
3. Observe the o/p waveform as shown in Fig 4(c), measure frequency of oscillations and the duty cycle and then sketch the o/p waveform.

Waveforms:

Monostable operation:

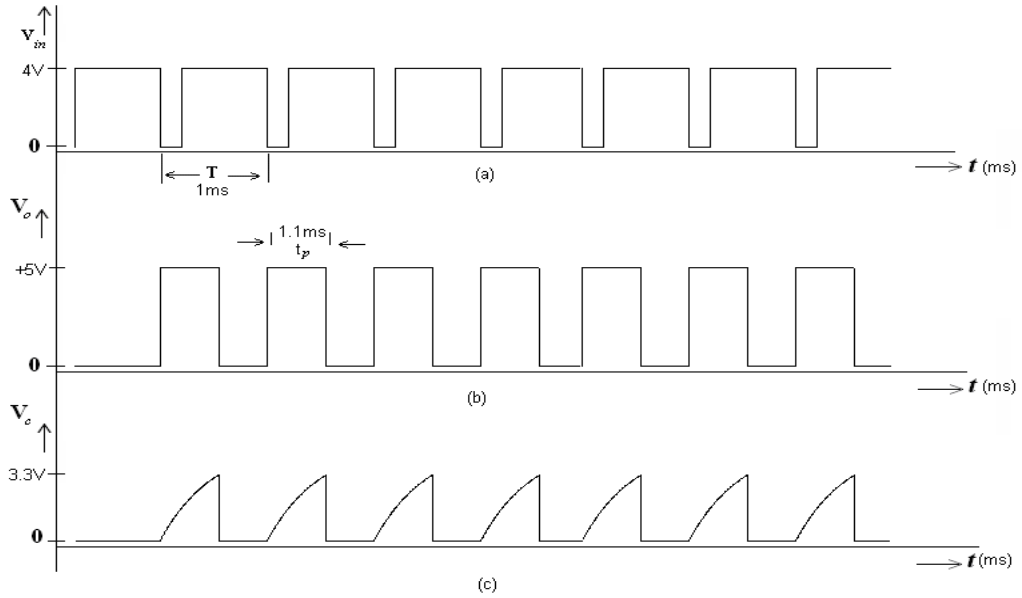


Fig 3 (a): Trigger signal (b): Output Voltage (c): Capacitor Voltage

Astable operation:

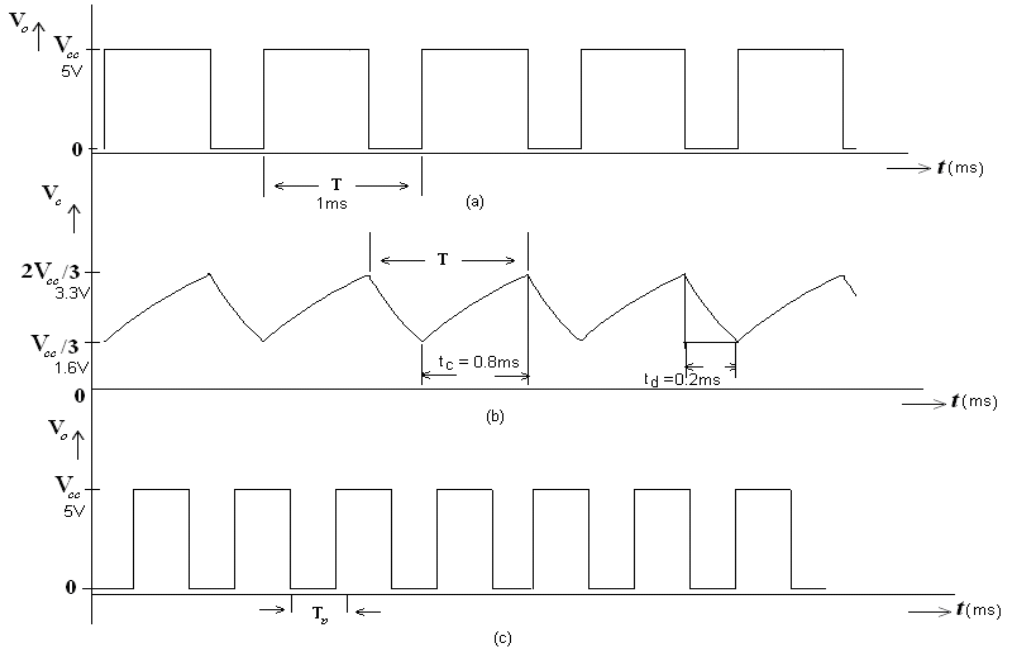


Fig 4 (a): Unsymmetrical square wave output

(b): Capacitor voltage of Unsymmetrical square wave output

(c): Symmetrical square wave output

Sample Readings:

Monostable operation:

Trigger	Output wave	Capacitor output
0 to 5V range 1)1V,0.09msec	0 to 5V range 4.6V, 0.5msec	0 to 3.33 V range 3V, 0.88 msec

Astable operation:

	Unsymmetrical	Symmetrical
Voltage V_{PP}	≈5V	≈ 5V
Time Period	0.1ms as T_C=0.08ms T_D=0.02ms	0.1ms as T_C = 0.05ms T_D = 0.05ms
Duty cycle	80%	50%

Precautions

Check the connections before giving the power supply.

Readings should be taken carefully.

Result:

The input and output waveforms of 555 timer monostable multivibrator are observed as shown in Fig 3(a), (b), (c).

Both unsymmetrical and symmetrical square waveforms are obtained and time period at the output is calculated in astable mode.

Inferences:

Output pulse width depends only on external components R_A and C connected to IC555.

Unsymmetrical square wave of required duty cycle and symmetrical square waveform can be generated.

Experiment No: 12

Title: PLL Using 1C 565

Aim: To study the operation of PLL using NE/SE 565.

Apparatus:

- 1C chip NE/SE 565.
- CRO.
- Signal generator
- 0.001 U.F, 1 u,F capacitors.
- 6.8KΩ resistor

Procedure:

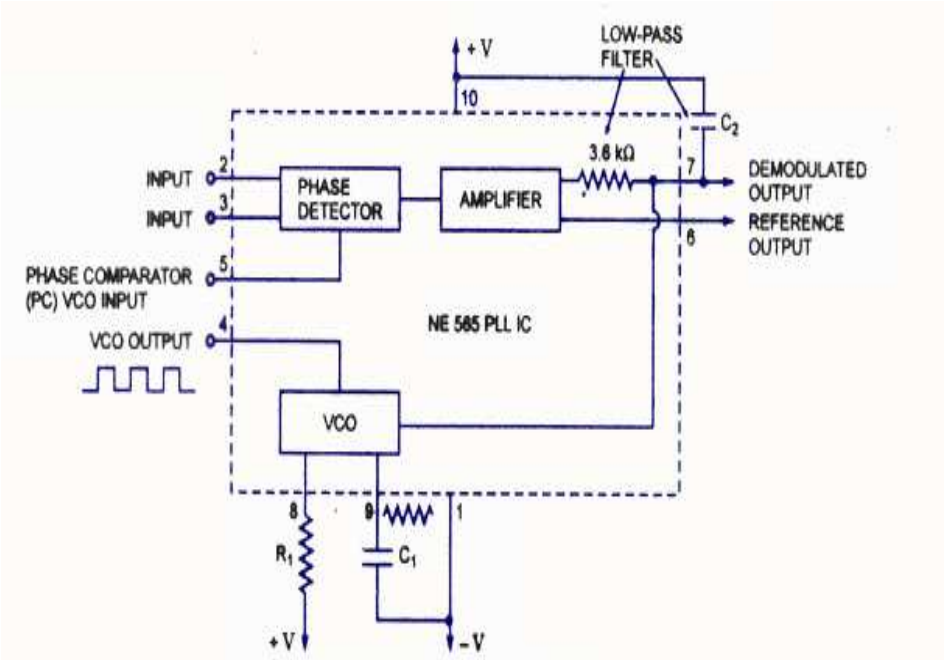
1. Make connections of the PLL as shown in fig
2. Measure the free running frequency of" VCO at pin 4.wilh the i/p signal V_{in}, set equal to zero. Compare it with the calculated value = $0.25/R_TC_T$
3. Now apply the i/p signal of 1 V_{PP}, square wave at a 1 KHz to pin 2.connect one channel of the scope to pin2 and display this signal on the scope.
4. Gradually increase the i/p frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower end of the capture range.Go on increasing the i/p frequency, till PLL tracks the i/p signal, say. to a frequency "f_2". This frequency "f_2" gives the upper end of the lock range. if i/p frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the i/p frequency till the PLL is again locked. This is the frequency (f_3) the upper end of the capture range. Keep on decreasing the i/p frequency until the loop is unlocked. This frequency 'f_4' gives lower end of lock range.
6. The lock range $\Delta f_L=f_2-f_4$. Compare it with the calculated value of $\pm 7.8f_o/12$.
   Also the capture range is $\Delta f_c= (f_3-f_1)$. Compare it with the calculated value of capture range.

Result:

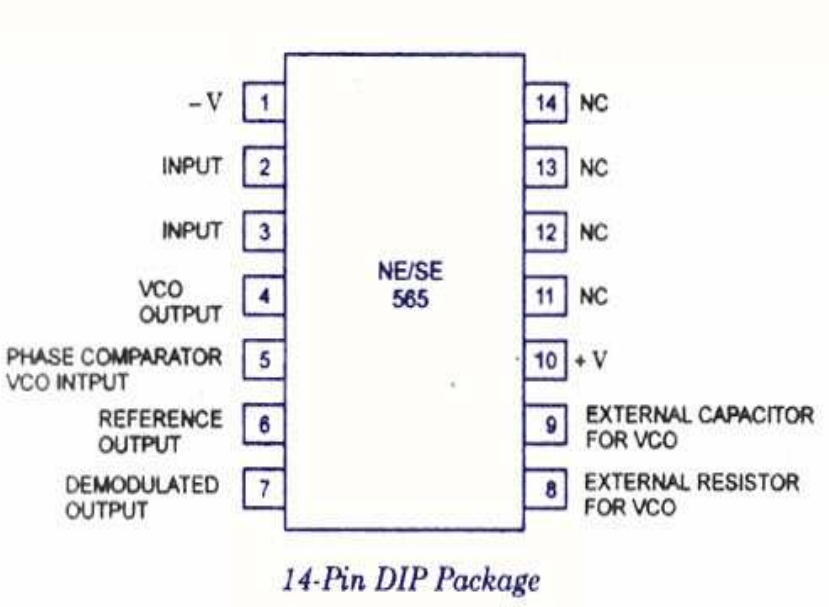
Theoretical values of lock range, capture range, free running frequency are compared with the practical values.

PLL applications:

1. Frequency multiplication /division
2. Frequency translation.
3. AM detection.
4. FM demodulation
5. FSK demodulator.



NE/SE 565 PLL Block Diagram



14-Pin DIP Package

13. IC723 Voltage Regulator

Aim: To design a low voltage variable regulator of 2 to 7V using IC 723.

Apparatus required:

S.No	Equipment/Component name	Specifications/Value	Quantity
1	IC 723	Refer appendix A	1
2	Resistors	3.3KΩ,4.7KΩ, 100 Ω	Each one
3	Variable Resistors	1KΩ, 5.6KΩ	Each one
4	Regulated Power supply	0 -30 V,1A	1

Theory:

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load current and input voltage variations. Using IC 723, we can design both low voltage and high voltage regulators with adjustable voltages.

For a low voltage regulator, the output V_O can be varied in the range of voltages $V_o < V_{ref}$, where as for high voltage regulator, it is $V_O > V_{ref}$. The voltage V_{ref} is generally about 7.5V. Although voltage regulators can be designed using Op-amps, it is quicker and easier to use IC voltage Regulators.

IC 723 is a general purpose regulator and is a 14-pin IC with internal short circuit current limiting, thermal shutdown, current/voltage boosting etc. Furthermore it is an adjustable voltage regulator which can be varied over both positive and negative voltage ranges. By simply varying the connections made externally, we can operate the IC in the required mode of operation. Typical performance parameters are line and load regulations which determine the precise characteristics of a regulator. The pin configuration and specifications are shown in the Appendix-A.

Circuit Diagram:

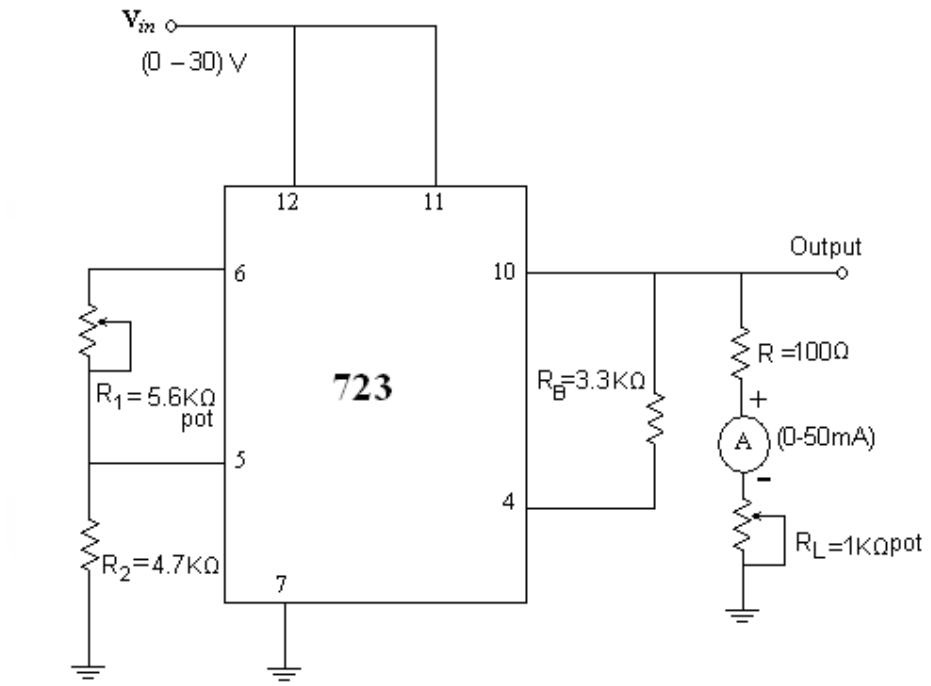


Fig1: Voltage Regulator

Design of Low voltage Regulator:

Assume I_o= 1mA,V_R=7.5V

R_B = 3.3 KΩ

For given V_o

$R_1 = (V_R – V_O) / I_o$

$R_2 = V_O / I_o$

Procedure:

a) Line Regulation*:*

1. Connect the circuit as shown in fig 1.
2. Obtain R_1 and R_2 for V_o=5V
3. By varying V_n from 2 to 10V, measure the output voltage V_o.
4. Draw the graph between V_n and V_o as shown in model graph (a)
5. Repeat the above steps for V_o=3V

b) Load Regulation*: For V_o=5V*

1. Set V_i such that V_O= 5 V
2. By varying R_L, measure I_L and V_o
3. Plot the graph between I_L and V_o as shown in model graph (b)

4. Repeat above steps 1 to 3 for V_O=3V.

Sample Readings

a) Line Regulation:

V_o set to 5V

Vi(V)	Vo(V)

Vo set to 3V

Vi(V)	Vo(V)

b) Load Regulation:

Vo set to 5V

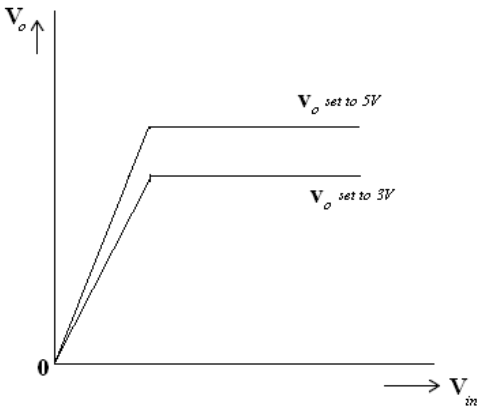
I_L (mA)	Vo(V)

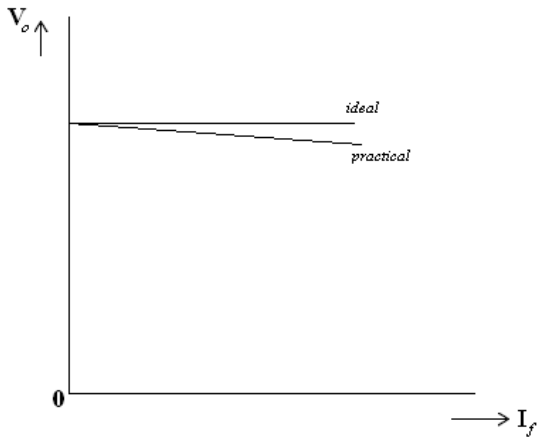
Vo set to 3V

I_L (mA)	Vo(V)

Model graphs:

a) Line Regulation **b) Load Regulation**





Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Results:

Low voltage variable Regulator of 2V to 7V using IC 723 is designed. The line and load regulation characteristics are plotted.

Inferences:

Variable voltage regulators can be designed by using IC 723.

Output varies linearly with input voltage up to some value(o/p voltage+ dropout voltage) and remains constant.

.

14.DESIGN OF VCO USING IC 566

Aim: i) To observe the applications of VCO-IC 566

ii) To generate the frequency modulated wave by using IC 566

Apparatus required:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	IC 566	Refer page no 10	1

2	Resistors	10KΩ 1.5KΩ	2 1
3	Capacitors	0.1 μF 100 pF	1 1
4	Regulated power supply	0-30 V, 1 A	1
5	Cathode Ray Oscilloscope	0-20 MHz	1
6	Function Generator	0.1-1 MHz	1

Theory: The VCO is a free running Multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a d.c control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "voltage controlled oscillator" or, in short, VCO.

The output frequency of the VCO can be changed either by R_1, C_1 or the voltage V_C at the modulating input terminal (pin 5). The voltage V_C can be varied by connecting a R_1R_2 circuit. The components R_1 and C_1 are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{CC} which can produce a frequency variation of about 10 to 1.

Circuit Diagram:

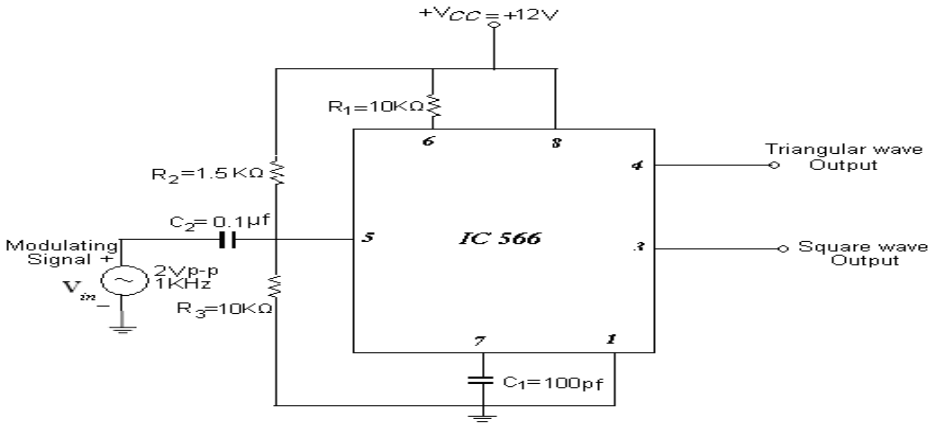


Fig1: Voltage Controlled Oscillator

Design:

1. Maximum deviation time period =T.
2. $f_{min} = 1/T$.
   where f_{min} can be obtained from the FM wave
3. Maximum deviation, $\Delta f = f_o - f_{min}$
4. Modulation index $\beta = \Delta f/f_m$
5. Band width $BW = 2(\beta+1) f_m = 2 (\Delta f+f_m)$
6. Free running frequency, $f_o = 2(V_{CC} - V_c) / R_1C_1V_{CC}$

Procedure:

1. The circuit is connected as per the circuit diagram shown in Fig1.
2. Observe the modulating signal on CRO and measure the amplitude and frequency of the signal.
3. Without giving modulating signal, take output at pin 4, we get the carrier wave.
4. Measure the maximum frequency deviation of each step and evaluate the modulating Index.

$m_f = \beta = \Delta f/f_m$

Waveforms:

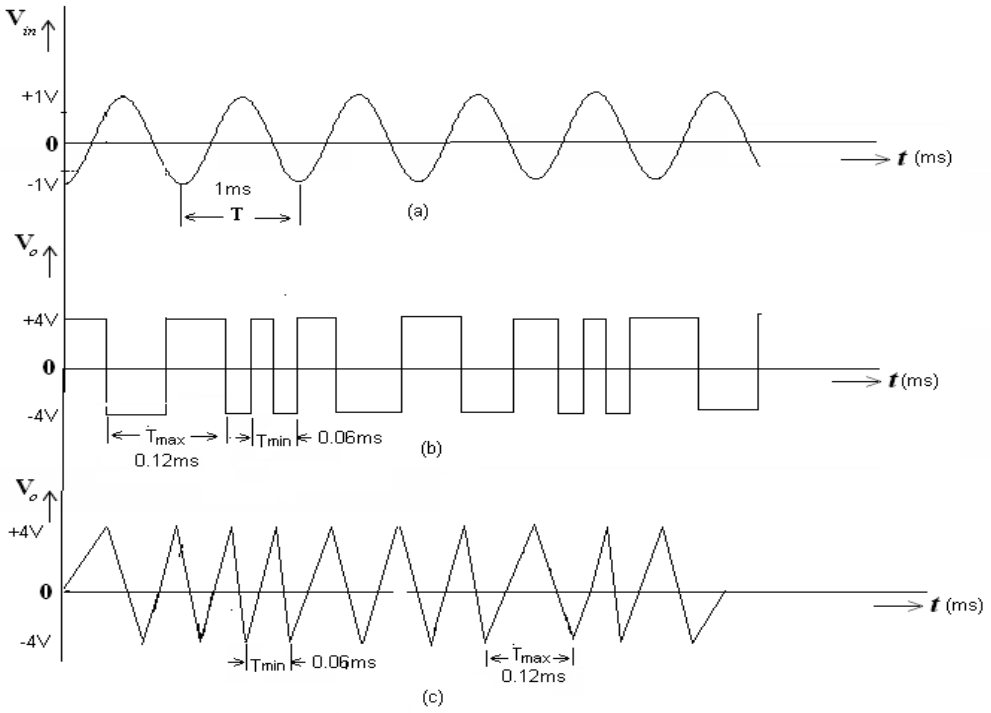


Fig 2 (a): Input wave of VCO

(b): Output of VCO at pin3

(c): Output of VCO at pin4

Sample readings:

V_{CC}=+12V; R_1=R_3=10KΩ; R_2=1.5KΩ; f_m=1KHz

Free running frequency, f_o = 26.1KHz

f_{min} = 8.33KHz

Δf= 17.77 KHz

$\beta = \Delta f/f_m$ = 17.77

Band width BW ≈ 36 KHz

Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Result:

Frequency modulated waveforms are observed and modulation Index, B.W required for FM is calculated for different amplitudes of the message signal.

Inferences:

During positive half-cycle of the sine wave input, the control voltage will increase, the frequency of the output waveform will decrease and time period will increase. Exactly opposite action will take place during the negative half-cycle of the input as shown in Fig (b).

15. 4 bit DAC using OP AMP

Aim: To design 1) weighted resistor DAC

2) R-2R ladder Network DAC

Apparatus required:

S.No	Equipment/Component name	Specifications/Value	Quantity
1	741 IC	Refer page no 2	1
2	Resistors	1KΩ,2KΩ,4KΩ, 8KΩ	Each one

3	Regulated Power supply	0-30 V , 1A	1
4	Multimeter(DMM)		1
5	connecting wires		
6	Digital trainer Board		1

Theory: Digital systems are used in ever more applications, because of their increasingly efficient, reliable, and economical operation with the development of the microprocessor, data processing has become an integral part of various systems Data processing involves transfer of data to and from the micro computer via input/output devices. Since digital systems such as micro computers use a binary system of ones and zeros, the data to be put into the micro computer must be converted from analog to digital form. On the other hand, a digital-to-analog converter is used when a binary output from a digital system must be converted to some equivalent analog voltage or current. The function of DAC is exactly opposite to that of an ADC.

A DAC in its simplest form uses an op-amp and either binary weighted resistors or R-2R ladder resistors. In binary-weighted resistor op-amp is connected in the inverting mode, it can also be connected in the non inverting mode. Since the number of inputs used is four, the converter is called a 4-bit binary digital converter.

Circuit Diagrams:

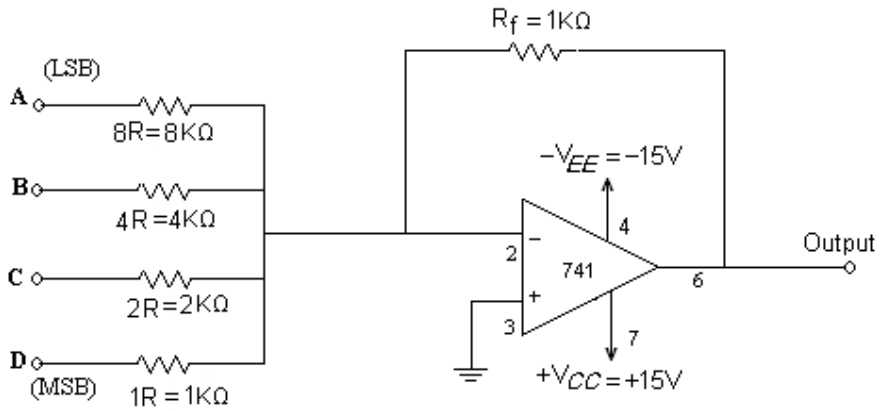


Fig 1: Binary weighted resistor DAC

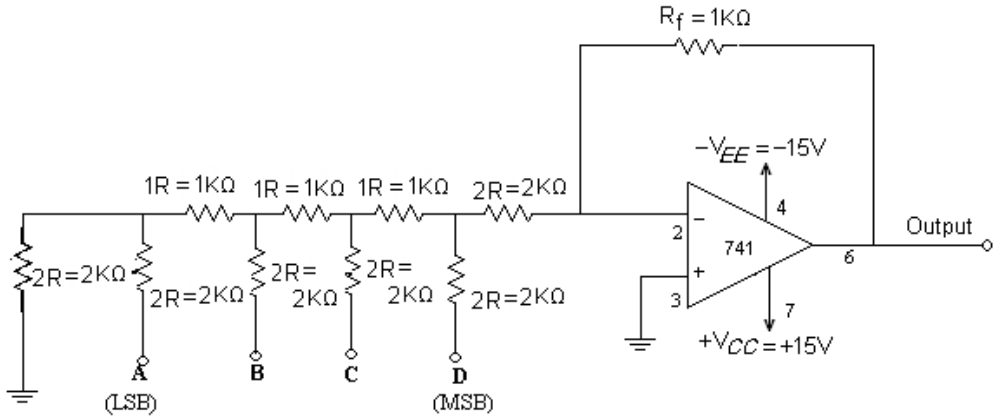


Fig 2: R – 2R Ladder DAC

Design:

1. Weighted Resistor DAC

$$V_o = -R_f \left[\frac{b_A}{8R} + \frac{b_B}{4R} + \frac{b_c}{2R} + \frac{b_D}{R} \right]$$

For input 1111, $R_f = R = 4.7K\Omega$

$$V_o = - \left[\frac{1}{8} + \frac{1}{4} + \frac{1}{2} + 1 \right] \frac{R_f}{R} x5$$

$V_o = - 9.375$ V

2.R-2R Ladder Network:

$$V_o = -R_f \left[\frac{b_A}{16R} + \frac{b_B}{8R} + \frac{b_c}{4R} + \frac{b_D}{2R} \right] \text{ X } 5$$

For input 1111, $R_f = R = 1K\Omega$

Procedure:

1. Connect the circuit as shown in Fig 1.
2. Vary the inputs A, B, C, D from the digital trainer board and note down the output at pin 6. For logic ‘1’, 5 V is applied and for logic ‘0’, 0 V is applied.
3. Repeat the above two steps for R – 2R ladder DAC shown in Fig 2.

Observations:

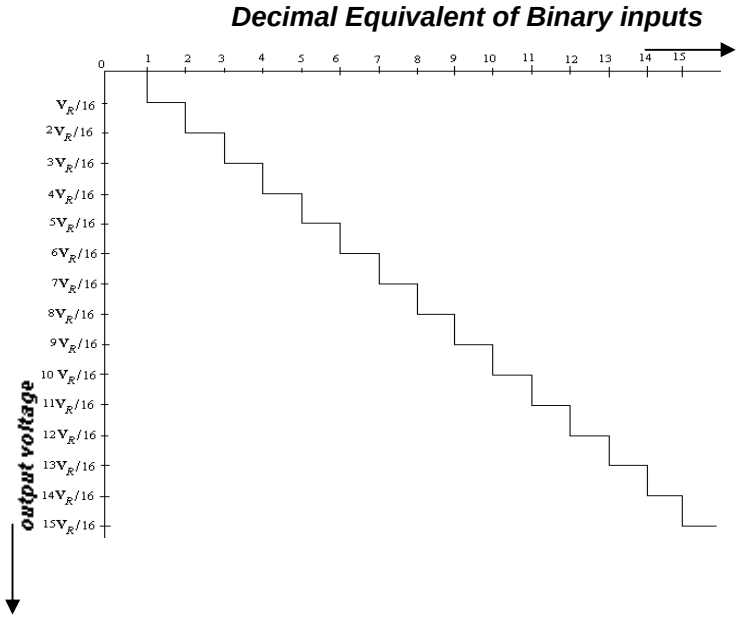
Weighted resistor DAC

S.No	D	C	B	A	Theoretical Voltage(V)	Practical Voltage(V)

R-2R Ladder Network:

S.No	D	C	B	A	Theoretical Voltage(V)	Practical Voltage(V)

Model Graph:



Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Results:

Outputs of binary weighted resistor DAC and R-2R ladder DAC are observed.

APPENDIX – A

BC107

Specifications:

1. Type : Si – NPN
2. operating point temp : 65^o to 200^oC
3. I_C(max) : 100mA
4. h_{fe} (min) = 110 : 100
5. h_{fe} (max) : 450
6. V_{CE} (max) : 45V
7. P_{tot}(max) : 300mW
8. Category(typical use) : Audio, low power

9. Possible substitutes :BC182, BC547

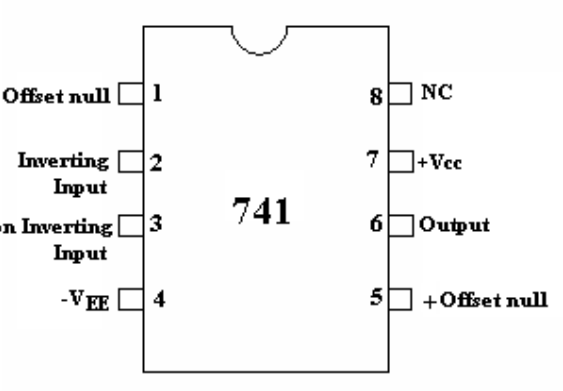
Diode

Type No	1N4007
Max. Peak Inverse Volts	50
Max RMS Supply Volts	35
Maximum Forward Voltage @ 1Ampere, DC @ 75^0 C	1.1 Volts,Peak
Maximum Reverse DC Current @PIV @ 25^0 C	10μA
Maximum Dynamic Reverse Current @PIV @75^0 C	30μA,Average

APPENDIX – B

IC 741

Pin Configuration:



Specifications:

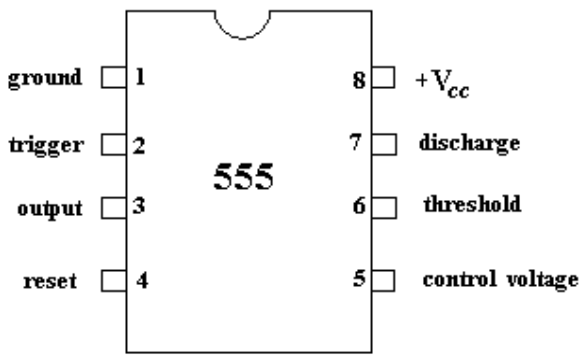
1. Voltage gain A = α typically 2,00,000
2. I/P resistance R_L = α Ω, practically 2MΩ

3. O/P resistance R_1 =0, practically 75Ω
4. Bandwidth = α Hz. It can be operated at any frequency
5. Common mode rejection ratio = α
   (Ability of op amp to reject noise voltage)
6. Slew rate + α V/µsec
   (Rate of change of O/P voltage)
7. When $V_1 = V_2$, V_D=0
8. Input offset voltage (Rs ≤ 10KΩ) max 6 mv
9. Input offset current = max 200nA
10. Input bias current : 500nA
11. Input capacitance : type value 1.4PF
12. Offset voltage adjustment range : ± 15mV
13. Input voltage range : ± 13V
14. Supply voltage rejection ratio : 150 µr/V
15. Output voltage swing: + 13V and – 13V for R_L > 2KΩ
16. Output short-circuit current: 25mA
17. supply current: 28mA
18. Power consumption: 85MW
19. Transient response: rise time= 0.3 µs
    Overshoot= 5%

APPENDIX – C

IC 555

Pin Configuration:



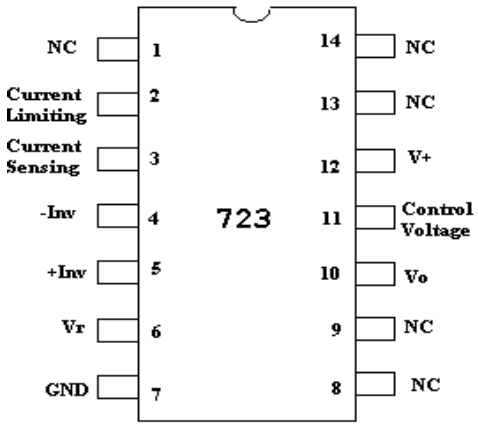
Specifications:

1.	Operating temperature	:	SE 555 -55^{o}C to 125^{o}C NE 555 0^{o} to 70^{o}C
2.	Supply voltage	:	+5V to +18V
3.	Timing	:	µSec to Hours
4.	Sink current	:	200mA
5.	Temperature stability	:	50 PPM/^{o}C change in temp or 0-005% /^{o}C.

APPENDIX – D

IC723

Pin Configuration:



Specifications of 723:

Power dissipation	:	1W
Input Voltage	:	9.5 to 40V
Output Voltage	:	2 to 37V
Output Current	:	150mA for Vin-Vo = 3V
		10mA for Vin-Vo = 38V
Load regulation	:	0.6% Vo
Line regulation	:	0.5% Vo

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